VMM1

Overview and Modes of Operation

VMM1 is the first prototype of a 64-channel front-end ASIC designed to operate with micropattern gas detectors. The ASIC provides charge amplification, analog filtering, discrimination , extraction of amplitude and timing (with neighbor channels), multiplexing. It also provides real time address of the first hit and direct timing output for a selected number of channels. The design, currently implementing an analog/digital interface, is expected to evolve into a version which includes ADCs and a fully-digital interface. Modes of operation are:

- Acquisition: events are detected and processed (amplitude and timing)
  - charge amplification, filtering, discrimination, peak- and time-detection
  - address in real time (ART) of the first event
  - direct timing (over-threshold or to peak) available for channels 0-7 and 56-63
- Readout: events are read out in sparse mode with smart token passing (amplitude, timing, address)
- Configuration: global and channel registers are accessible for configuration
- Operation controlled with pins *ena, wen, ck, di, do, tki, tko, stp* as described in section *Pinout and Controls*.
- All digital IOs are **custom LVDS** at 600mV +/- 150mV

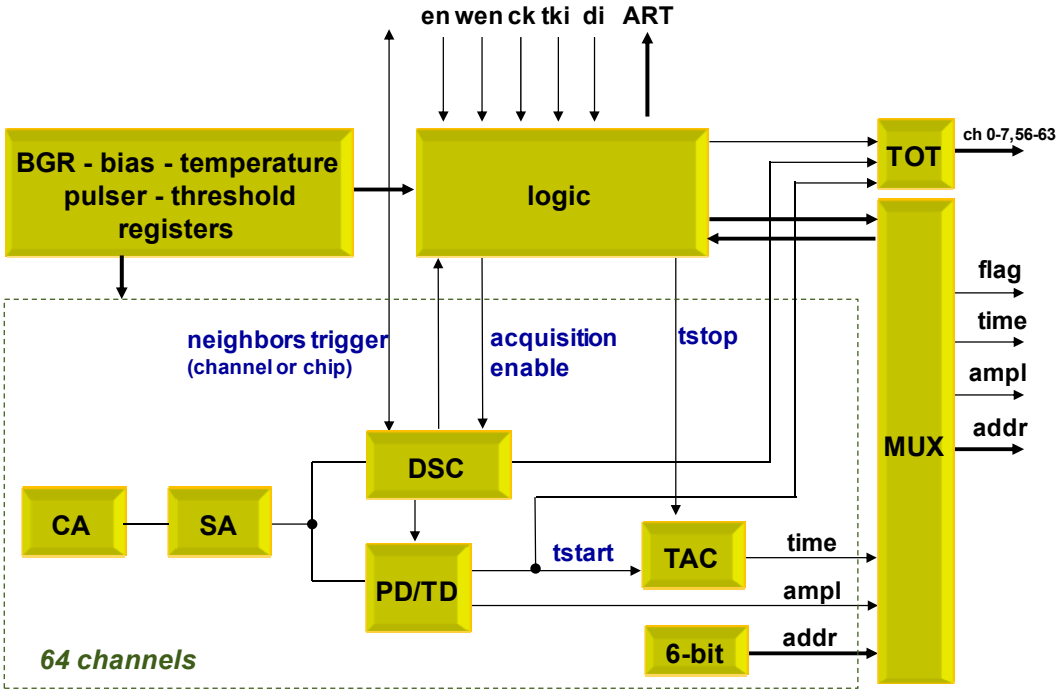


Fig. 1 - ASIC block diagram

Technology, Specifications, Functionalities

- **Technology**: CMOS 130nm 1.2V from IBM (8RF)
- **Layout size, device count**: : 5.934 x 8.433 = 50.033 mm², 500k MOSFETs, 80k capacitors, 200k resistors
- **Power dissipation**: 1.2 V x 300 mA = ~ 360 mW (~5.5 mW/channel)

- **Analog front-end**
  - acceptable sensor capacitance: optimized for 200pF, can operate from sub pF to 400pF, optimization for >30pF with channel register bit *sc*.
  - input MOSFET: 10mm, 1.65mA, 18pF
  - acceptable input charge polarity: positive and negative, controlled with channel register bit *sp*.

- shaper: 3rd order with complex conjugate poles in Delayed Dissipative Feedback (DDF) configuration
- output baseline stabilizer
- peaking time adjustable: 25, 50, 100, 200 ns, controlled with global register bits *st0,st1*.
- gain adjustable: 0.5, 1, 3, 9 mV/fC (maximum charge 2, 1, 0.33, 0.11 pC), controlled with global register bits *sg0,sg1*.
- simulated charge resolution: ~ 5000e^- (1800e^-) at 25ns (100ns), 200pF
- simulated timing resolution: ~ 1ns at 1V signal amplitude.
- channel mask, enabled with channel register bit *sm*.
- test capacitor ~ 1.2pF, enabled with channel register bit *st*.
- input leakage generator (required for continuous reset), enabled with channel register bit *sl*.
- pulse generator, common to all channels, 10-bit adjustable, ~1mV steps, with global bit registers *sdp0-sdp9,* strobe with *di* input when in *acquisition mode*.

- **Signal processing**
  - amplitude discriminator capable of processing sub-hysteresis signals, sub-hysteresis enabled with global register bit *ssh*.
  - discrimination threshold adjustable with 10-bit global DAC, ~1mV steps, global register bits *sdt0-sdt9* and 4-bit channel DAC, ~1mV steps, channel register bits *sd0-sd3*.
  - option of disabling discrimination once the first peak is detected, enabled with global register bits *sdp*.
  - force-neighbor signal processing for above-threshold events: when an event exceeds the threshold, the neighbor channels (in neighbor chips if required) are forced to peak-detect mode; enabled with global register bit *sng*; first and last channels communicate with associated channels in neighbor chips through bi-directional pins *sett, setb.*
  - peak detector with peak-found signal for accurate timing (multi-phase: track, peak-detect, hold&buffer).
  - time detector at peak-found with time-to-amplitude conversion implementing voltage ramp with adjustable duration: 0.125, 0.25, 0.5, 1 µs, controlled with global register bits *stc0,stc1*; ramp starts at peak-found from peak detector and stops either at falling edge of *ena* input or at falling edge of *stp* input, depending on setting of global register bit *sstp*.
  - first-event address (Address in Real Time, ART) available at outputs *fa0-fa5* either at threshold crossing or at peak found with flag indicator at output *fflag* and self-resetting in 40ns, enabled and controlled with global register bits *sfa, sfam*.
  - time-over-threshold or time-to-peak direct timing outputs available for channels 0-7 and 56-67 at dedicated outputs *ttp0-ttp7* and *ttp56-ttp63*, (7 and 56 become neighbors) enabled and controlled with global register bits *sttt,stot,s16*.
- **Readout**
  - peak amplitude (from peak detector), peak timing (from time detector) and address stored in analog/digital memories, are multiplexed, buffered (buffers enabled with global register bits *sbfp,sbft*), and read out in sparse mode by using a smart token-passing logic where the token stops only at channels with events to readout (either above threshold or neighbors).
  - multiplexed analog outputs available at analog outputs *pdo, tdo*.
  - multiplexed addresses available at digital outputs *a0-a5* .
  - a *flag* is released when the first peak is found.
  - optional self-reset after 40ns from the *flag* signal.
  - smart resets allow resetting either the acquisition chain or the full ASIC (including the configuration registers) by a combining pulses and levels at *ena* and *wen* inputs.
- **Analog Monitors**
  - buffered (buffers enabled with global register bit *sbfm*) analog output *mo* to selectively monitor channel analog output, channel trimmed threshold, coarse threshold, pulse generator (after pulser switch), temperature sensor output, and band-gap reference output; controlled with global register bits *scmx, sm0-sm5* and channel register bit *smx*.
- **Configuration**
  - when in configuration mode, registers are accessible through *ck* and *di* inputs; the written configuration is available at the *do* output.
  - global register: 48 bits (two not used), channel register: 16-bits (six not used)

Registers

- **global bits (defaults are 0)**
  - *sg1,sg0 [00 01 10 11]*: gain (0.5, 1, 3, 9 mV/fC)(2, 1, 0.33, 0.11 pC)
  - *st1,st0 [00 01 10 11]*: peaktime (200, 100, 50, 25 ns)
  - *sng*: neighbor (channel and chip) triggering enable
  - *stc1,stc0 [00 01 10 11]*: TAC slope adjustment (125, 250, 500, 1000 ns)
  - *sdp*: disable-at-peak
  - *scmx, sm5-sm0*: monitor multiplexing
    - common monitor: *scmx, sm5-sm0 [0 000001 to 000100]*, pulser DAC (after pulser switch), threshold DAC, band-gap reference, temperature sensor
    - channel monitor: *scmx, sm5-sm0 [1 000000 to 111111]*, channels 0 to 63
  - *sfa [0 1], sfam [0 1]*: ART enable (*sfa [1]*) and mode (*sfam [0]* timing at threshold, *[1]* timing at peak)
  - *sbfm [0 1],sbfp [0 1],sbft [0 1]*: analog output buffers enable *[1]* (*mo*, *pdo*, *tdo*)
  - *sstp [0 1]*: TAC stop setting (*ena*-low *[0]* or *stp*-low *[1]*)
  - *ssh [0 1]*: sub-hysteresis discrimination enable *[1]*
  - *sttt [0 1],stot [0 1]*: timing outputs enable (*sttt [1]*) and mode (*stot [0]* time-over-threshold, *[1]* threshold-to-peak)
  - *s16 [0 1]*: makes ch7 neighbor to ch56 *[1]*
  - *srst [0 1]*: acquisition self resets about 40 ns after *flag [1]*
  - *sdt0-sdt9 [0:0 through 1:1]*: coarse threshold DAC
  - *sdp0-sdp9 [0:0 through 1:1]*: test pulse DAC
- **channel bits (defaults are 0)**
  - *sp [0 1]*: input charge polarity (*[0]* negative, *[1]* positive)
  - *sc [0 1]*: large sensor capacitance mode (*[0]* <~30pF, *[1]* >~30pF)
  - *sl [0 1]*: leakage generator enable *[1]*
  - *st [0 1]*: 1.2pF test capacitor enable *[1]*
  - *sm [0 1]*: mask enable *[1]*
  - *sd0-sd3 [0:0 through 1:1]*: trim threshold DAC, 1mV step (*[0:0]* trim 0V, *[1:1]* trim +15mV)
  - *smx [0 1]*: channel monitor mode (*[0]* analog output, *[1]* trimmed threshold)
- **bit order and configuration process**
  - enabled with *wen* high, data shifted at falling edge of *ck*, latched at *wen* low
  - single string, 48+16x64=1072 bit
  - global register:
    - [*sdp sstp srst sbft sbfp sbfm s16 sm5:sm0 scmx sfa sfam st1:0 sg1:0 sng stot sttt ssh stc1:0 sdt9:0 sdp9:0*]
  - channel register (64x):
    - [*sp sc sl st sm sd0:sd3 smx 0 0 0 0 0 0*]
  - first bit to write: channel 63 last bit
  - last bit to write: *sdp*

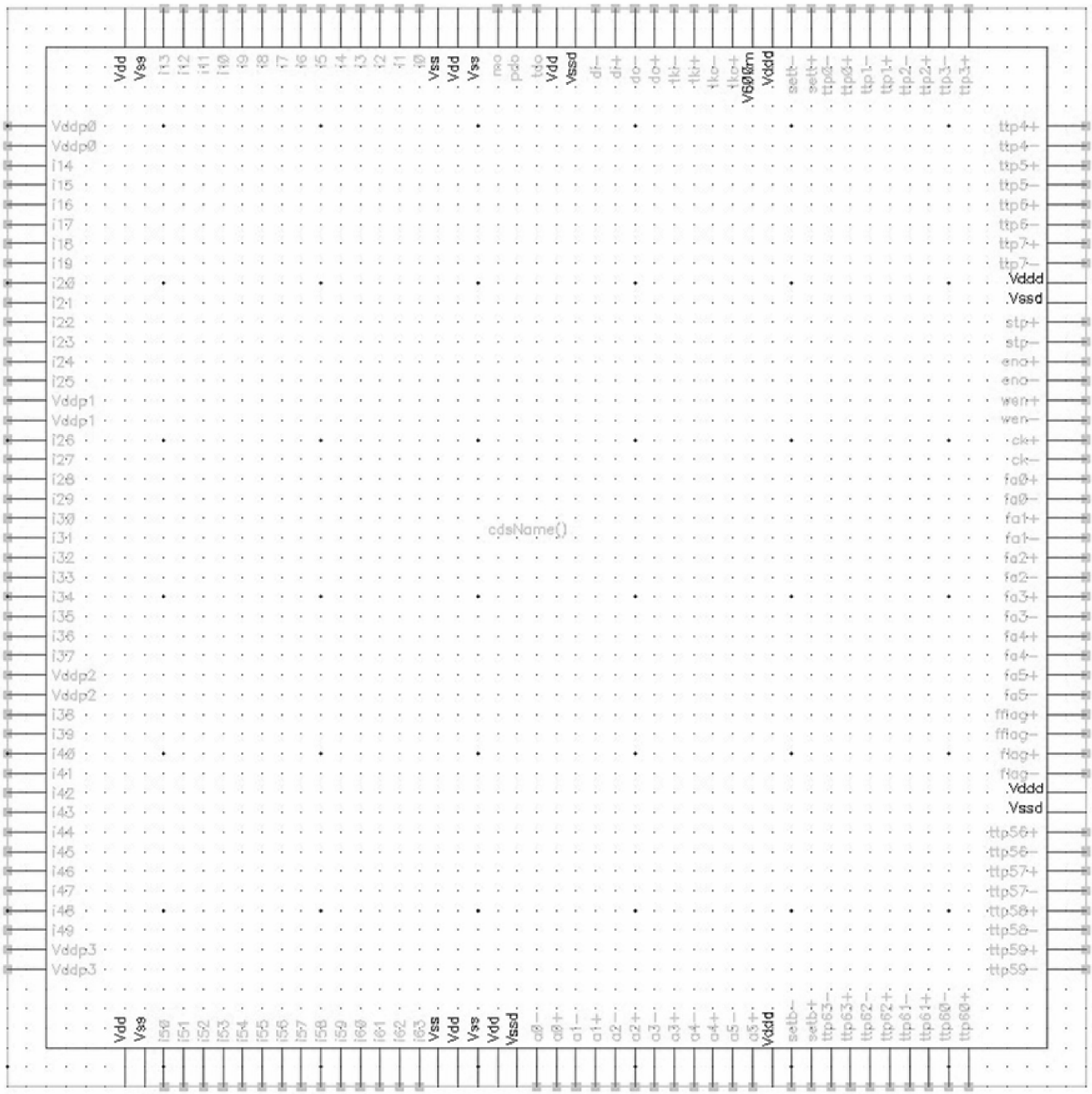
Pinout and Controls

- 176 pins (44 each side)
- *Vdd,Vss*: analog supplies 1.2V and grounds 0V
- *Vddd, Vssd*: digital supplies 1.2V and grounds 0V
- *Vddp0-Vddp3*: charge amplifier supplies 1.2V
- *V600m*: reference for LVDS 600mV
- *i0-i63*: analog inputs, ESD protected
- *mo*: monitor multiplexed analog output
- *pdo*: peak detector multiplexed analog output
- *tdo*: time detector multiplexed analog output

- *flag*: event indicator
- *a0-a5*: multiplexed address output, tristated (driven with token)
- *ttp0-ttp7* and *ttp56-ttp63*: time-over-threshold or time-to-peak digital outputs
- *fflag*: ART event indicator
- *fa0-fa5*: ART address output
- *sett*: ch0 neighbor trigger
- *setb*: ch63 neighbor trigger

- ***ena***: acquisition enable
  - *ena* high, *wen* low: acquisition mode
    - internally enabled after 40ns from *ena* high
  - *ena* low, *wen* low: readout mode
  - *ena* pulse, *wen* high: global reset (acquisition and registers)
- ***wen***: configuration enable
  - *wen* high: configuration mode
  - *wen* pulse: acquisition reset
- ***ck***: clock
  - in acquisition mode *ck* is timing counter clock (not used in this version)
  - in readout mode *ck* is readout clock
  - in configuration mode *ck* is writein clock
- ***di, do***: data configuration input and output (1/2 clock shifted)
  - in acquisition *di* becomes pulser clock
- ***tki, tko***: token input and output (3/2 clock wide)
- ***stp***: timing stop

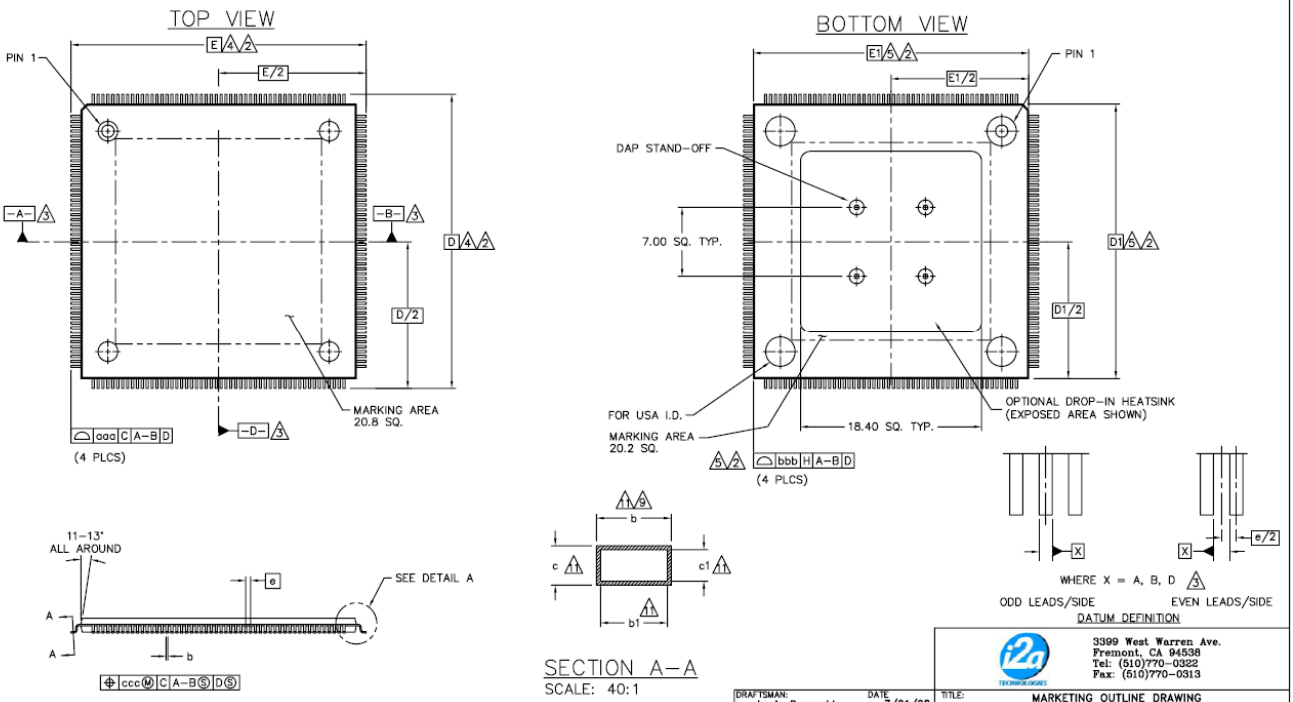
Pinout



Package

LQFP208A

REVISION HISTORY			
ECN #	REV	DATE	DESCRIPTION
96-030	A	07/25/96	NEW DRAWING
	B	7/01/98	STAND-OFF(A,A1), CALL-OUT(D,D1,E,E1)ETC. ADD HEATSINK FIGURE
	C	08/11/98	ADD 256 LD, UPDATE NOTES & SPEC.



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DRAFTSMAN: Louie Rezonable	DATE 7/01/98	TITLE: MARKETING OUTLINE DRAWING 28 X 28 X 1.4mm LQFP UNIVERSAL DIE UP/DOWN	
CHECKER: Dennis Leung	DATE 8/11/98		
APPROVED:	DATE	DRAWING NO.: QFP-MPO-28T-XXX-01	REV. C
APPROVED:	DATE		PAGE: 1/2 SCALE:

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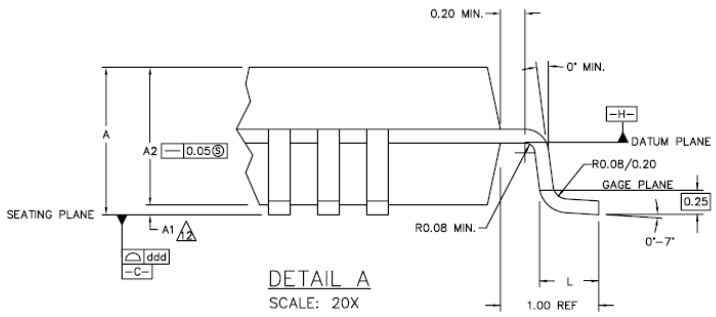

SYMBOL	LEAD COUNT; FOOT PRINT 160; 2.0 FP			NOTE
	MIN.	NOM.	MAX.	
A	===	===	1.60	
A1	0.05	===	0.15	
A2	1.35	1.40	1.45	
D		30.00 BSC		
D1		28.00 BSC		
E		30.00 BSC		
E1		28.00 BSC		
L	0.45	0.60	0.75	
e		0.65 BSC		
b	0.22	===	0.38	
b1	0.22	0.28	0.33	
c	0.09	===	0.20	
c1	0.09	===	0.16	
	Tolerances of form and position			
aaa		0.20		
bbb		0.20		
ccc		0.12		
ddd		0.08		

SYMBOL	LEAD COUNT; FOOT PRINT 208; 2.0 FP			NOTE
	MIN.	NOM.	MAX.	
A	===	===	1.60	
A1	0.05	===	0.15	
A2	1.35	1.40	1.45	
D		30.00 BSC		
D1		28.00 BSC		
E		30.00 BSC		
E1		28.00 BSC		
L	0.45	0.60	0.75	
e		0.50 BSC		
b	0.17	===	0.27	
b1	0.17	0.22	0.24	
c	0.09	===	0.20	
c1	0.09	===	0.16	
	Tolerances of form and position			
aaa		0.20		
bbb		0.20		
ccc		0.08		
ddd		0.08		

SYMBOL	LEAD COUNT; FOOT PRINT 256; 2.0 FP			NOTE
	MIN.	NOM.	MAX.	
A	===	===	1.60	
A1	0.05	===	0.15	
A2	1.35	1.40	1.45	
D		30.00 BSC		
D1		28.00 BSC		
E		30.00 BSC		
E1		28.00 BSC		
L	0.45	0.60	0.75	
e		0.40 BSC		
b	0.13	===	0.23	
b1	0.13	0.16	0.19	
c	0.09	===	0.20	
c1	0.09	===	0.16	
	Tolerances of form and position			
aaa		0.20		
bbb		0.20		
ccc		0.07		
ddd		0.08		

NOTES:

1. ALL DIMENSIONS ARE IN MM. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1994.
2. FOR DIE DOWN PACKAGE, THE TOP PACKAGE BODY IS SHOWN IN BOTTOM VIEW AND THE LEADS ARE FORMED UPSIDE DOWN.
3. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
4. TO BE DETERMINED AT SEATING PLANE -C-.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. SURFACE FINISH OF THE PACKAGE IS #24-27 CHARMILLE (1.6-2.3 $\mu m R_a$). PIN 1 AND EJECTOR PIN MAY BE LESS THAN 0.1 $\mu m R_a$.
7. DAMBAR REMOVAL: PROTRUSION DOES NOT EXCEED 0.08. INTRUSION DOES NOT EXCEED 0.03.
8. BURR: BURR DOES NOT EXCEED 0.08 IN ANY DIRECTION.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 FOR 0.40 AND 0.50 PITCH PACKAGE.
10. CORNER RADIUS OF PLASTIC BODY DOES NOT EXCEED 0.20.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
13. FINISH OF LEADS IS 85% TIN 15% LEAD, OR 100% TIN PLATED.
14. ALL SPECIFICATIONS AND DIMENSIONS ARE SUBJECTED TO i2a TECHNOLOGIES MANUFACTURING PROCESS FLOW AND MATERIALS.
15. THE PACKAGES DESCRIBED IN THIS DRAWING CONFORM TO JEDEC MS-026D. WHERE DESCREPANCIES BETWEEN THE JEDEC AND i2a TECHNOLOGIES DOCUMENTS EXIST, THIS DRAWING WILL TAKE THE PRECEDENCE.

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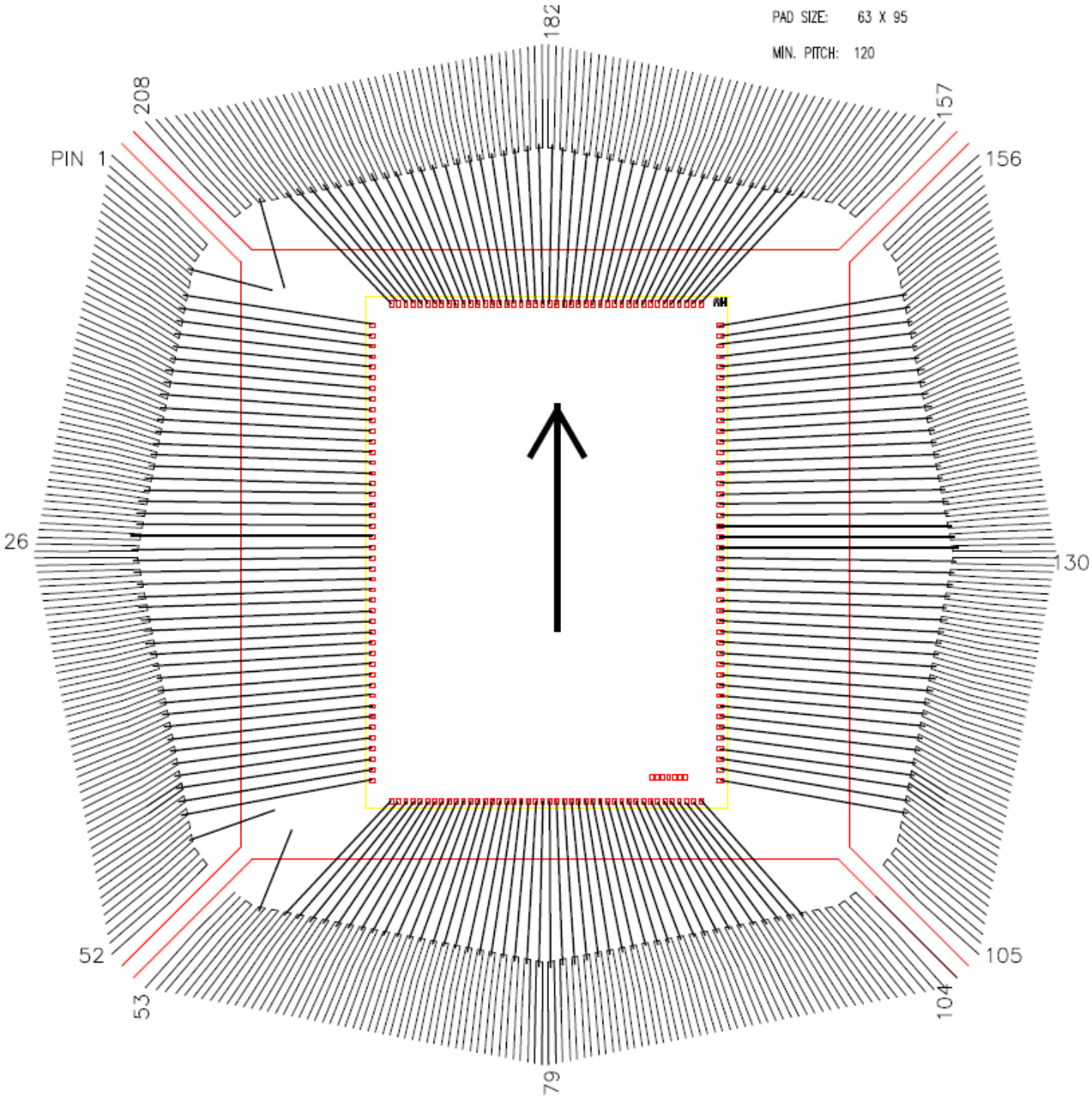
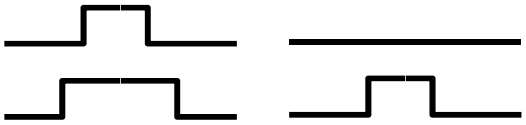
Bonding Diagram

LQFP208A

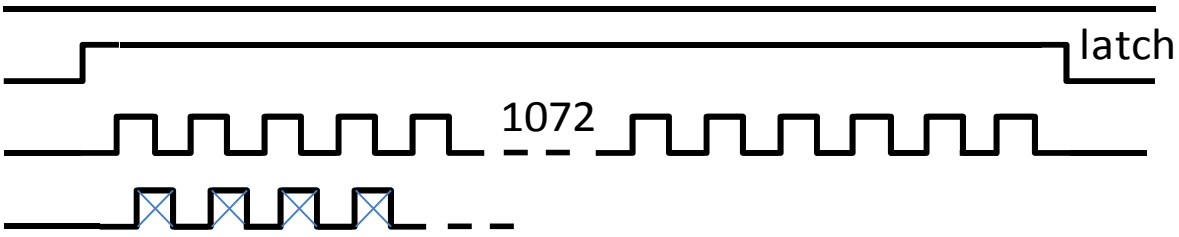


Timing Diagrams

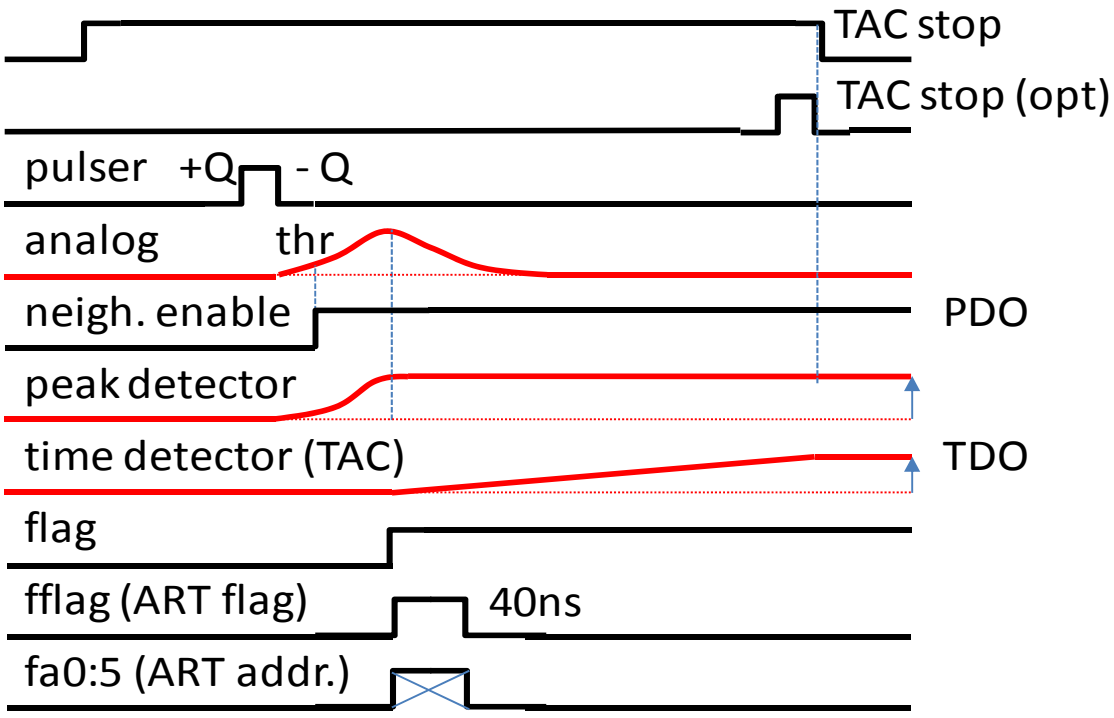
- **Global reset (acquisition and registers) and acquisition reset**
  - ena
  - wen



- **Configuration**
  - ena
  - wen
  - ck
  - di



- **Acquisition (typical, direct timing outputs not shown)**
  - ena
  - stp
  - di
  - set
  - flag
  - fflag
  - fa0:5



- **Readout (typical)**
  - tki
  - ck
  - flag
  - a0:a5