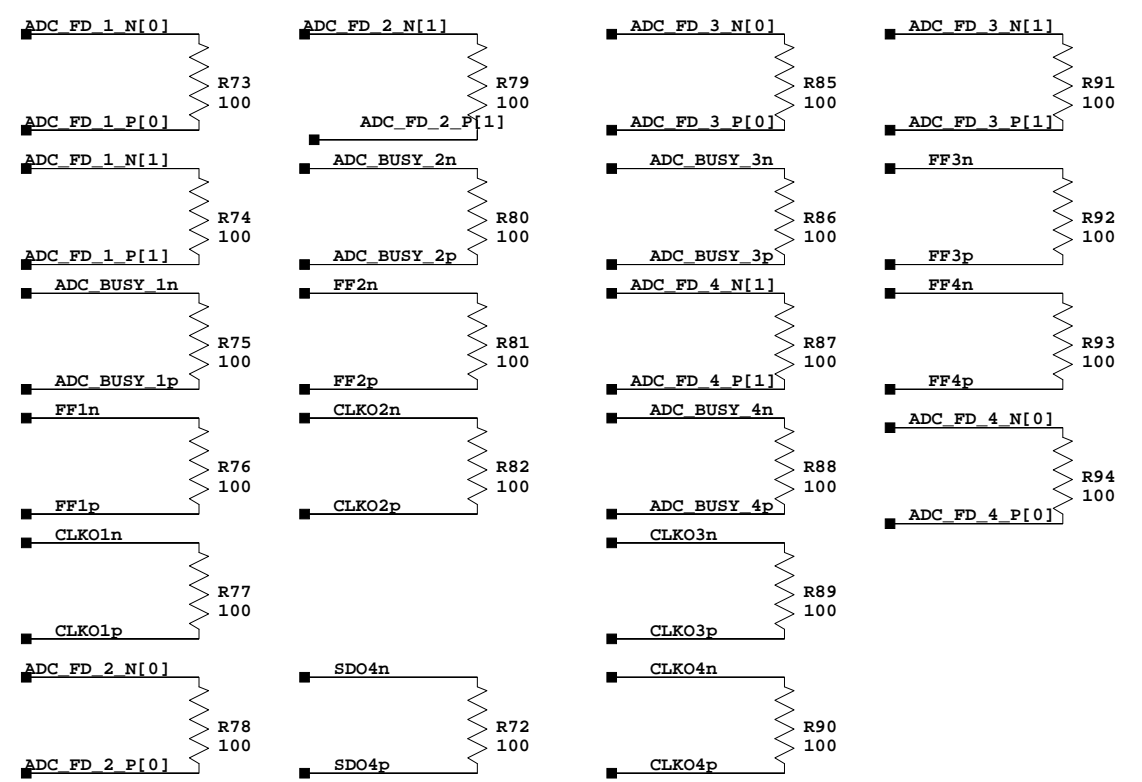
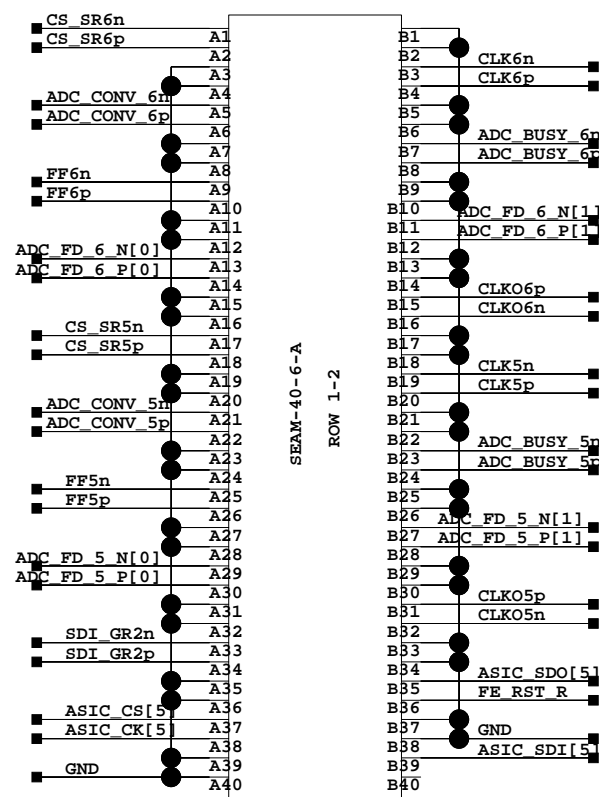


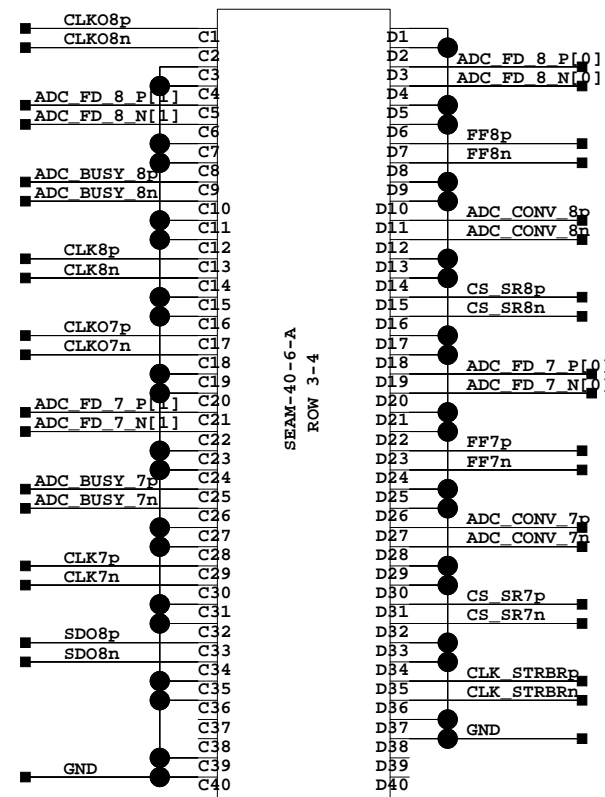
**LVDS TERMINATION  
PLACE UNDER FPGA**





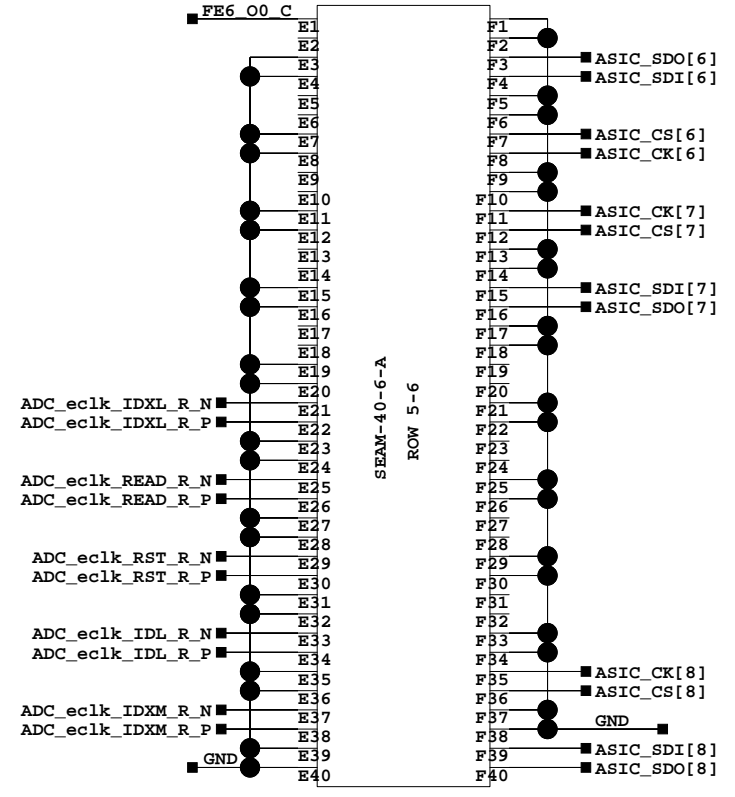
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ROW 1-2

P2



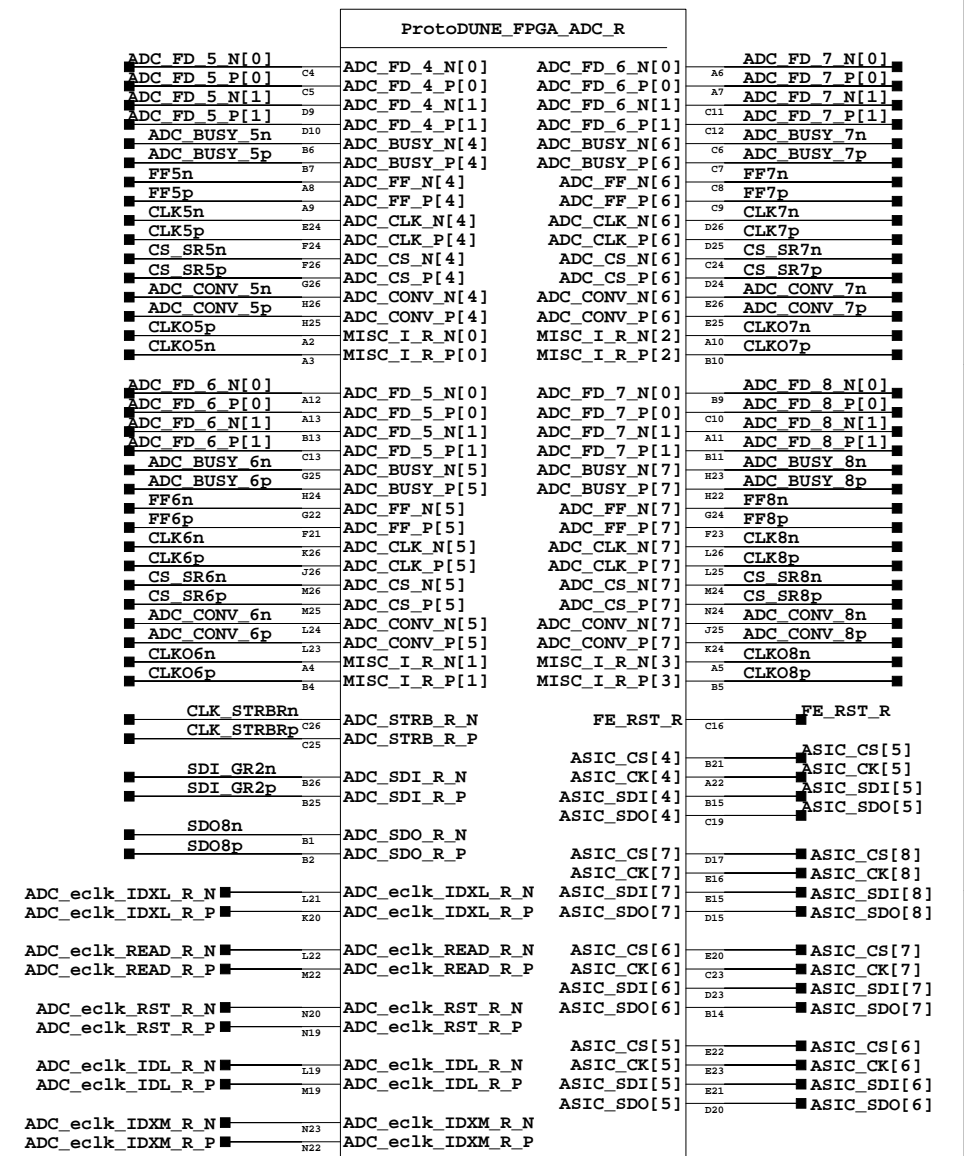
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ROW 3-4

P2



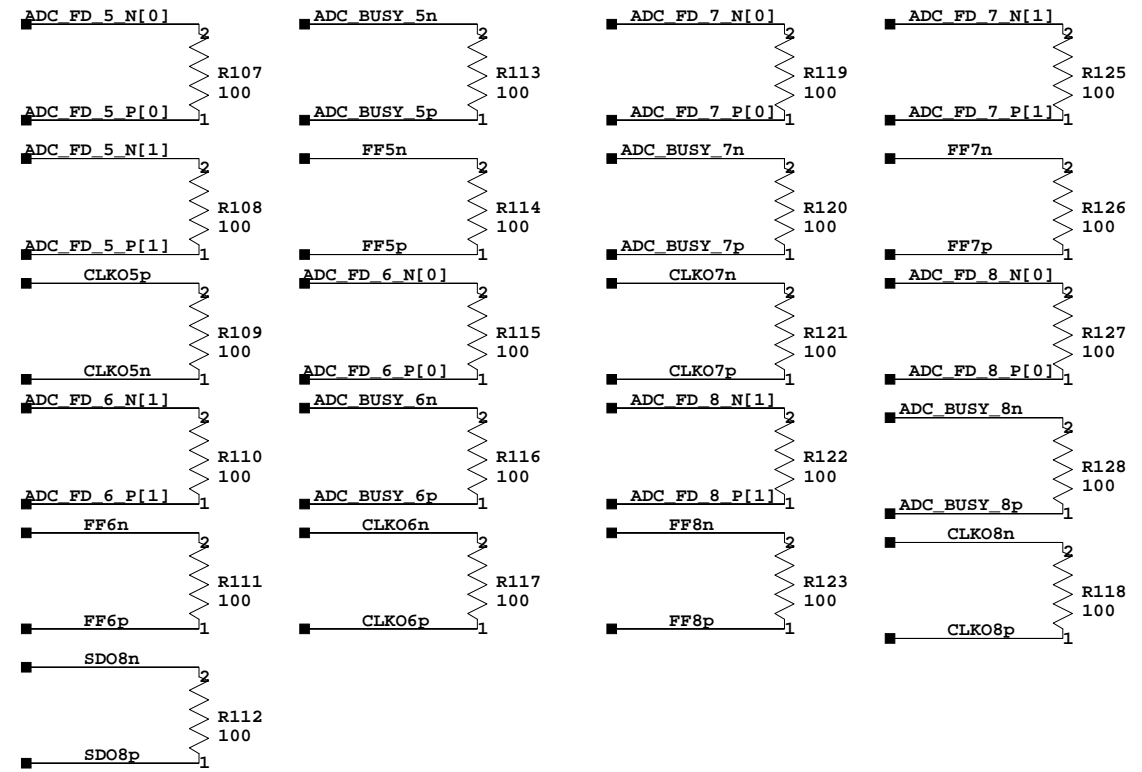
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ROW 5-6

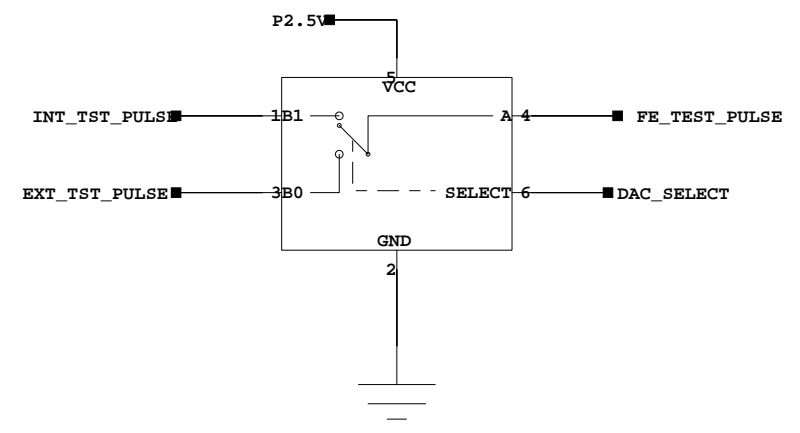
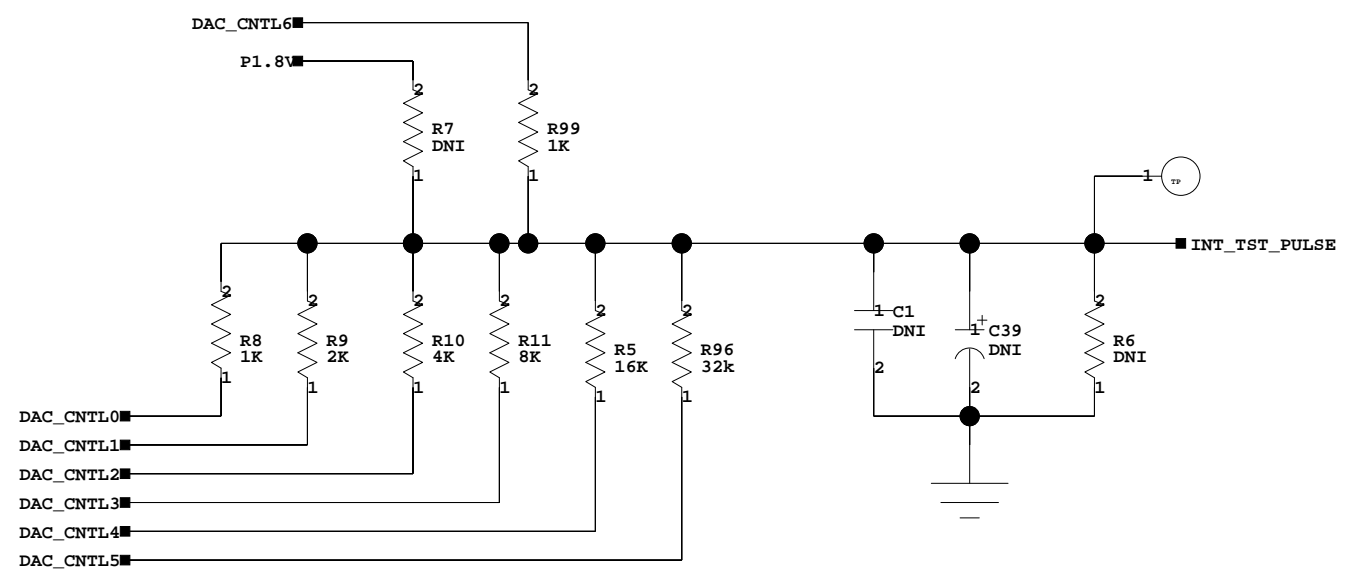
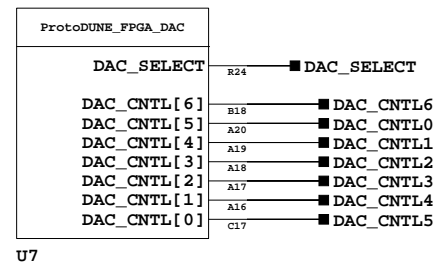
P2



U7

### LVDS TERMINATION PLACE UNDER FPGA



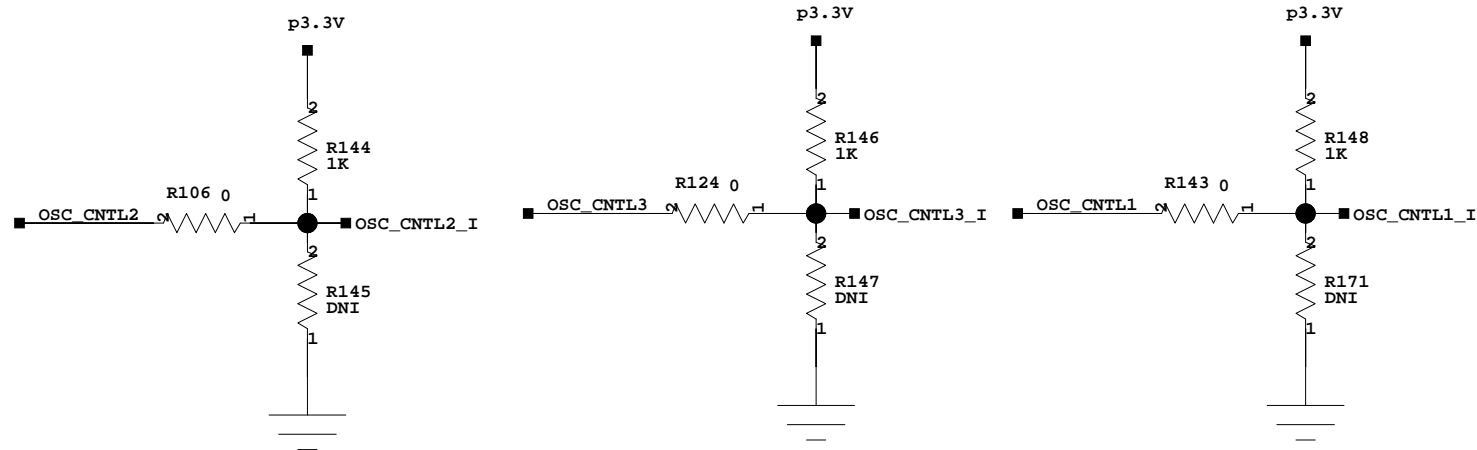
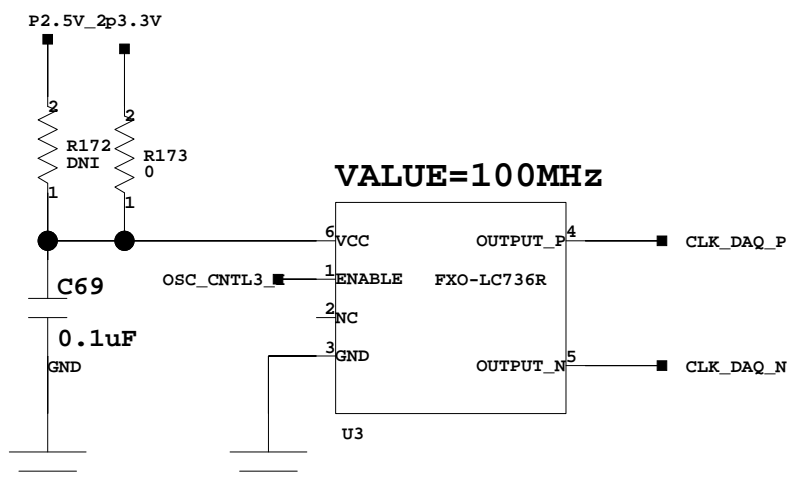
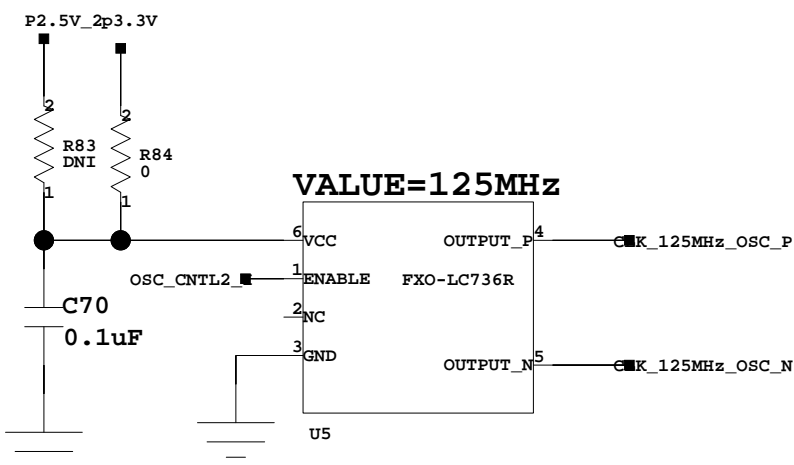
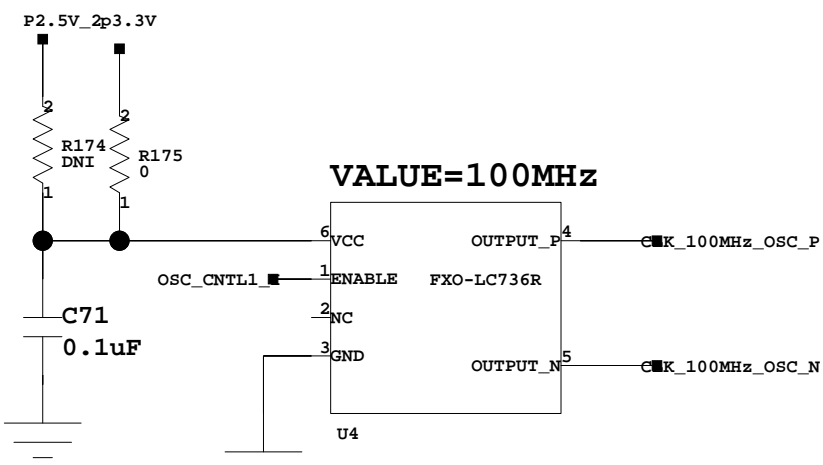


A

B

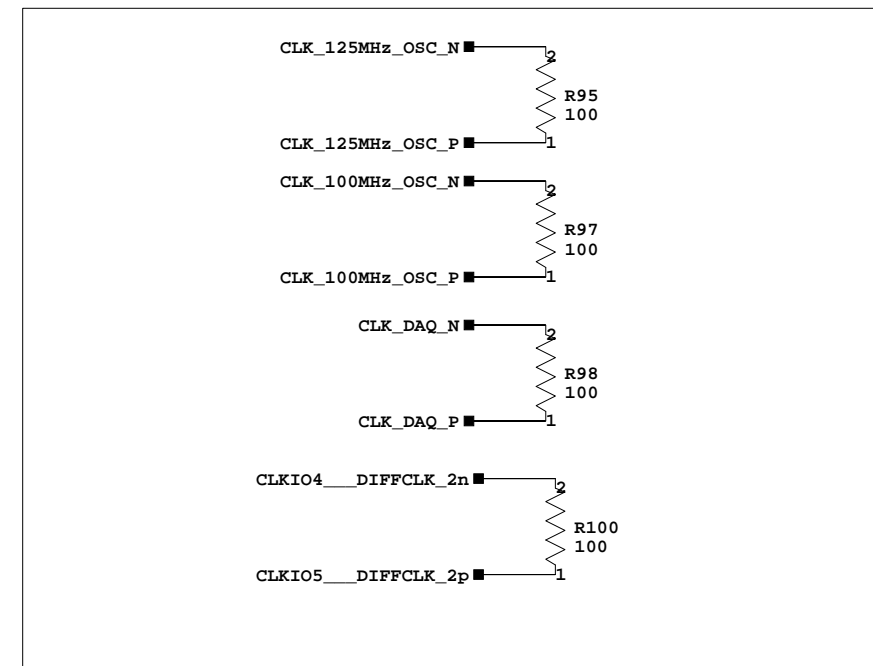
C

D



ProtoDUNE_FPGA_CLK		
SBND_CLK	U9	CLK_GXB_100MHz_N
SBND_CLK	T9	CLK_GXB_100MHz_P
CLK_125MHz_OSC_N	K9	CLK_UDP_125MHz_N
CLK_125MHz_OSC_P	L9	CLK_UDP_125MHz_P
CLK_100MHz_OSC_N	T15	CLK_100MHz_OSC_N
CLK_100MHz_OSC_P	T14	CLK_100MHz_OSC_P
CLK_DAQ_N	N26	CLK_DAQ_N
CLK_DAQ_P	N25	CLK_DAQ_P
CLK_DAQ_N	L14	CLK_EXT_N
CLK_DAQ_P	L15	CLK_EXT_P
CLK_100MHz_OSC_N	K10	REFCLK4n
CLK_100MHz_OSC_P	L10	REFCLK4p
I2C_SCL_DIF	U10	REFCLK1n
I2C_SCL_DIF	T10	REFCLK1p
CLKIO4_DIFFCLK_2n	P26	CLKIO4_DIFFCLK_2n
CLKIO5_DIFFCLK_2p	R26	CLKIO5_DIFFCLK_2p

U7



UNDER FPGA

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DUNE\_CLK

Date: 11/08/2017:10:53

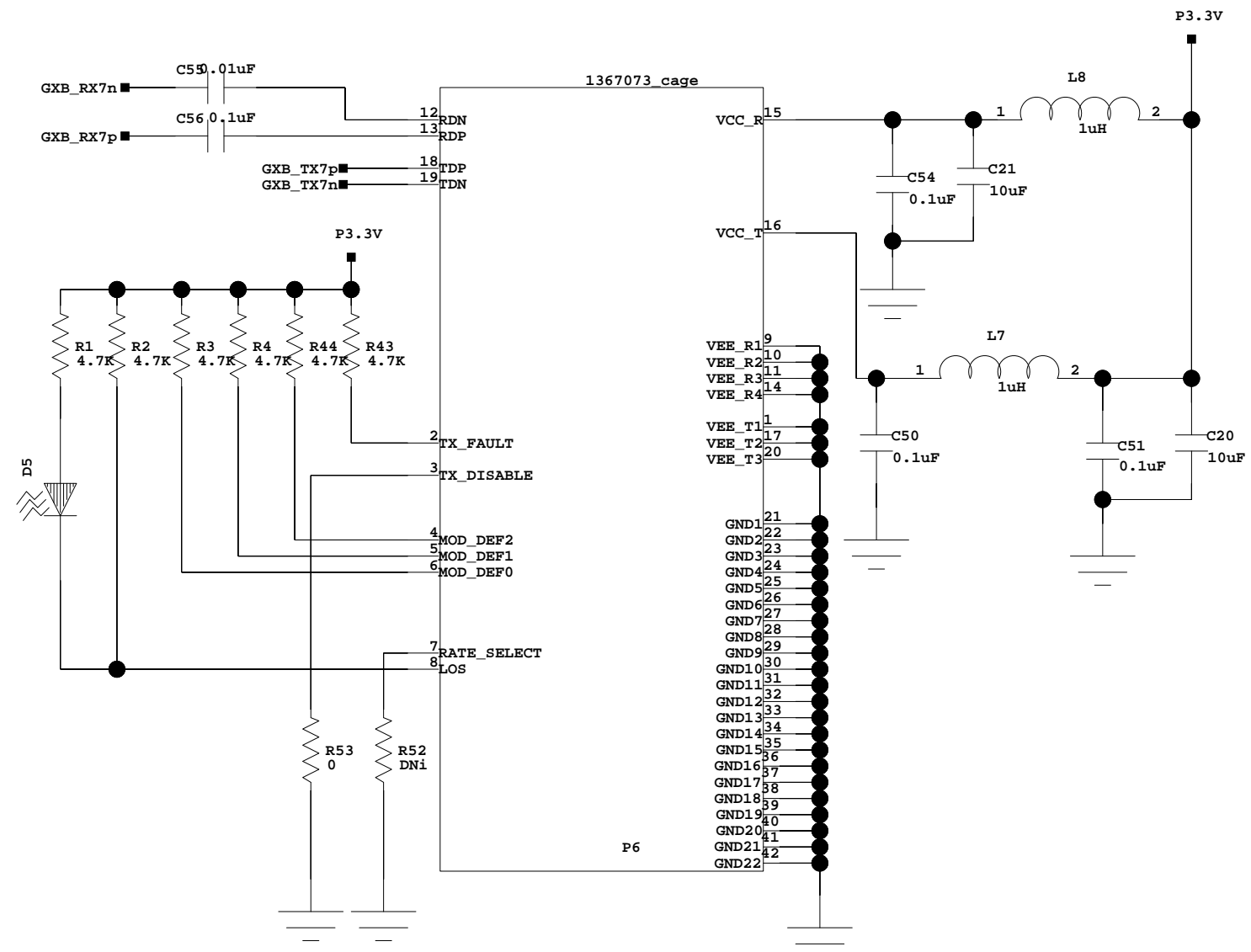
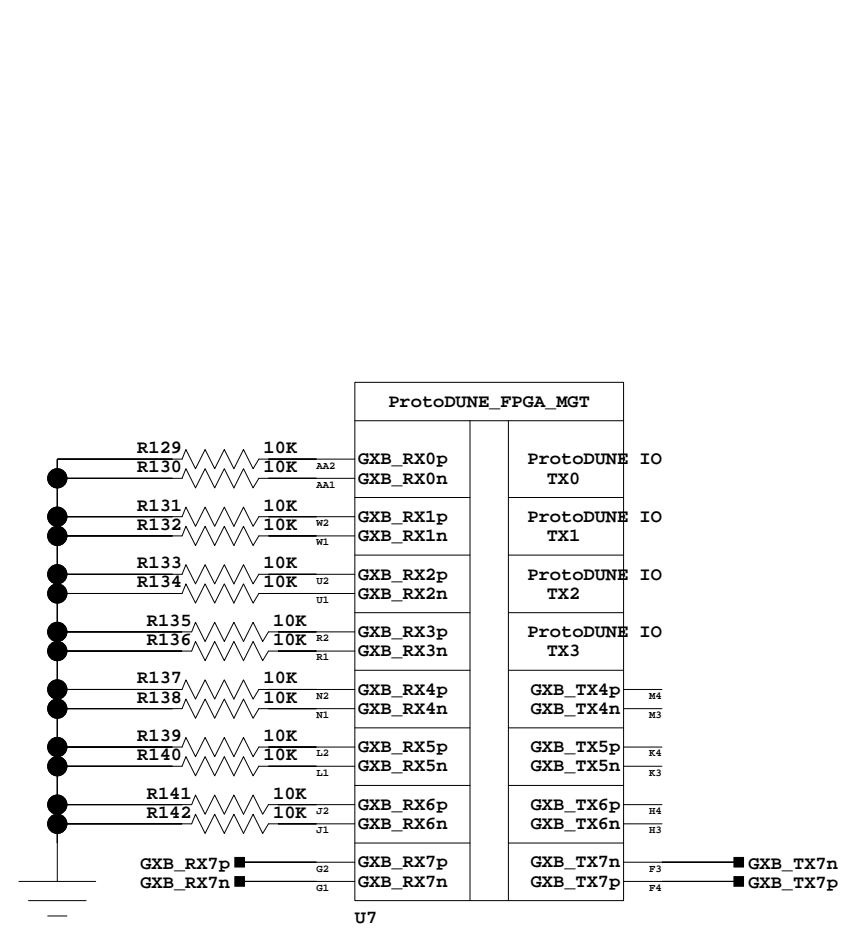
DRAWN BY: Jack Fried

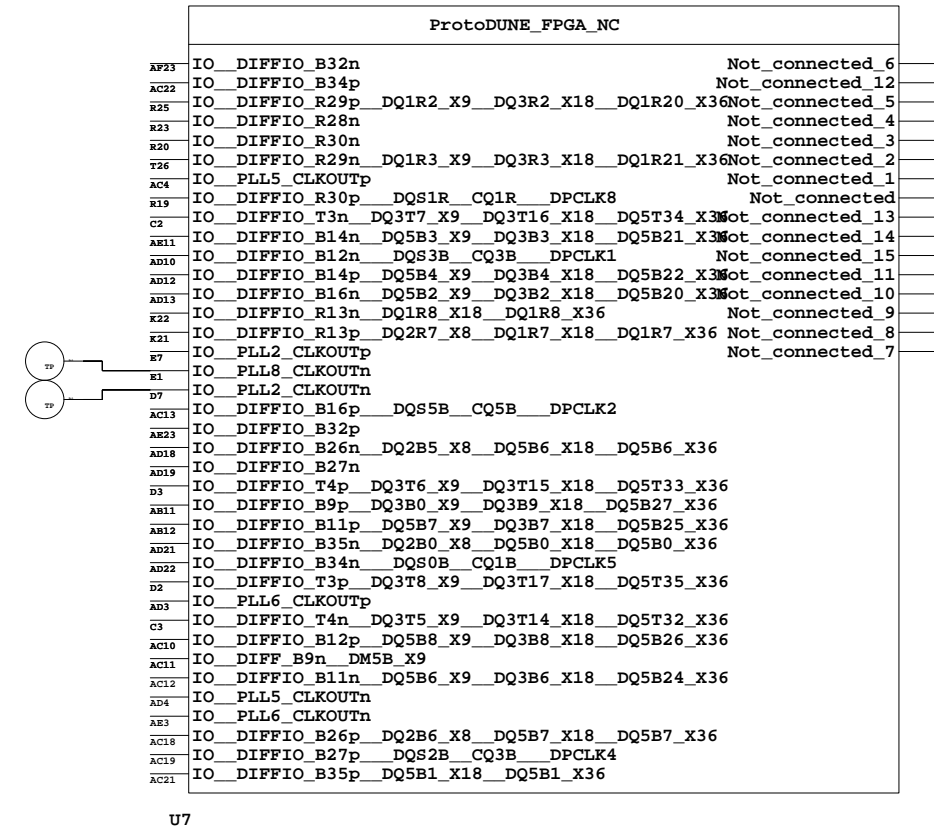
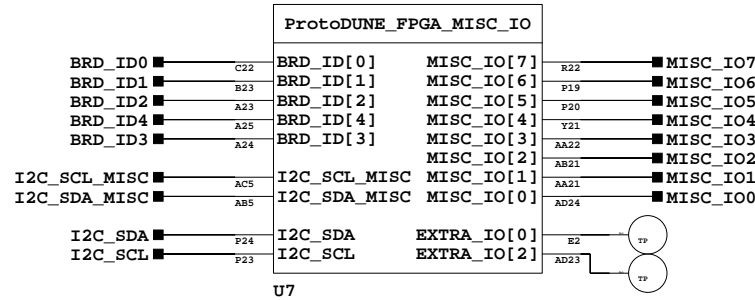
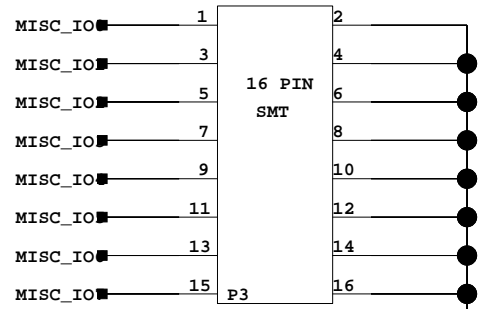
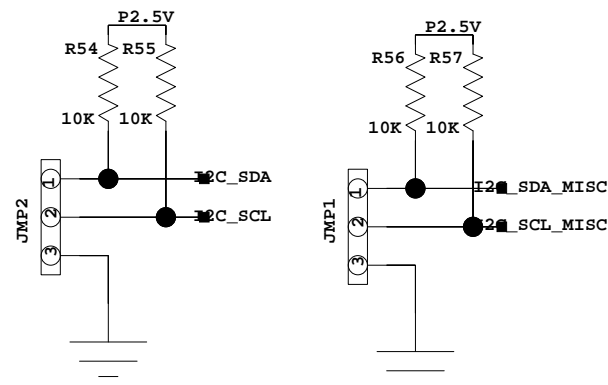
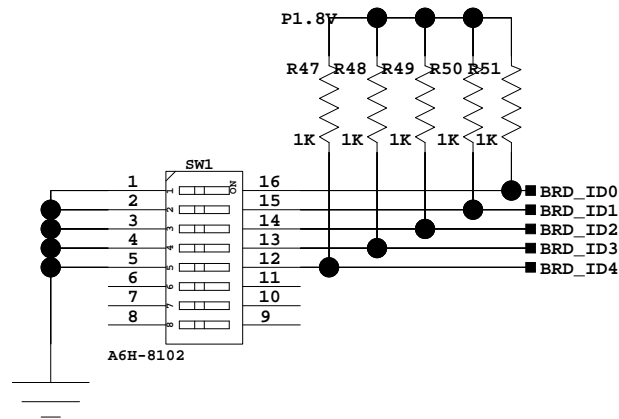
A

B

C

D



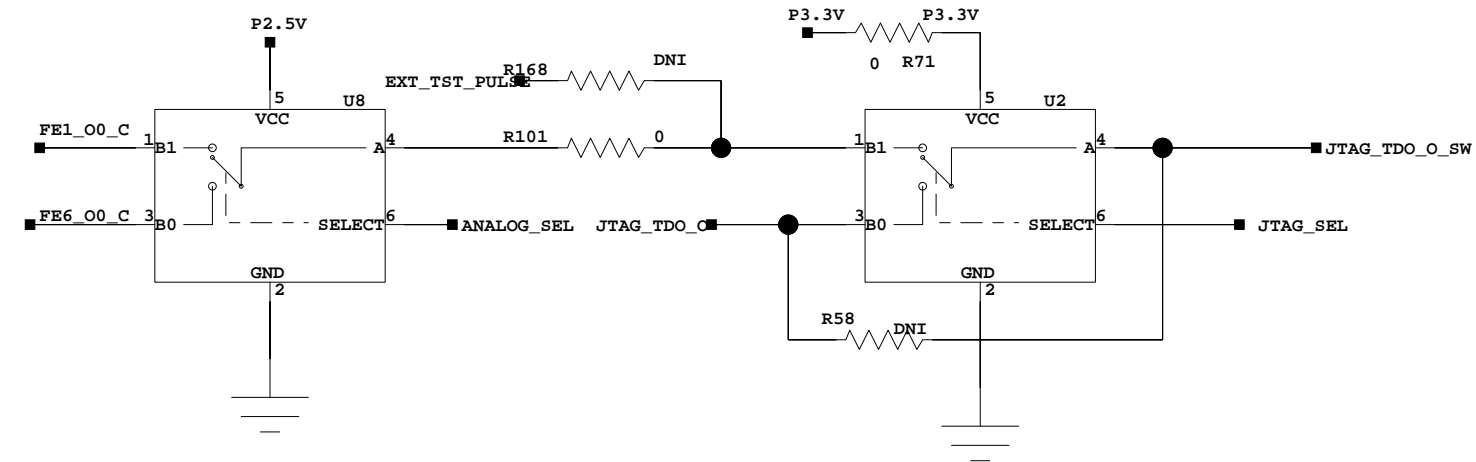
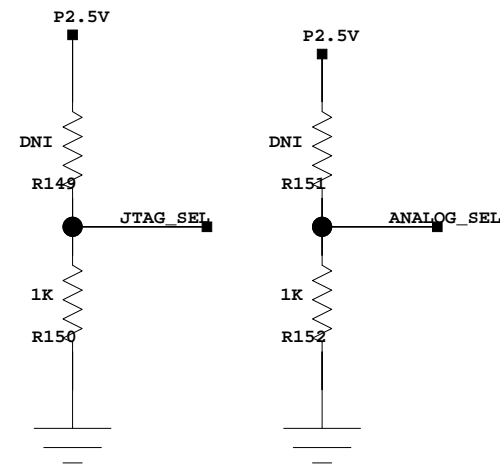
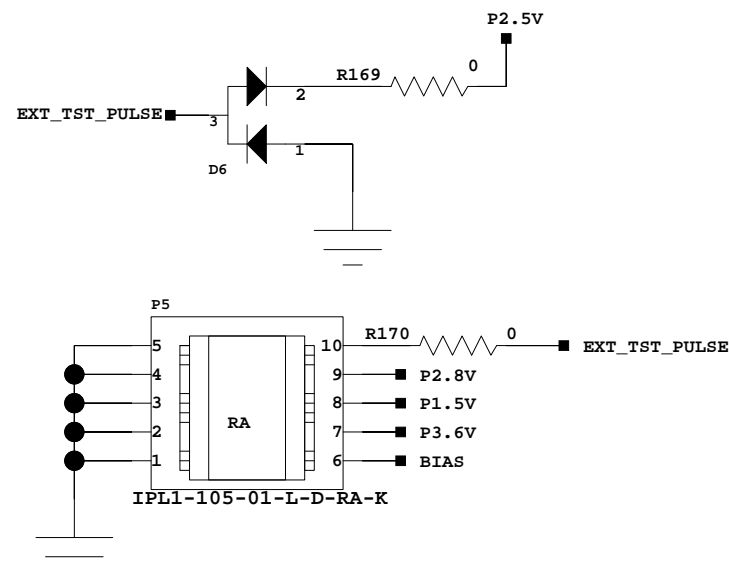


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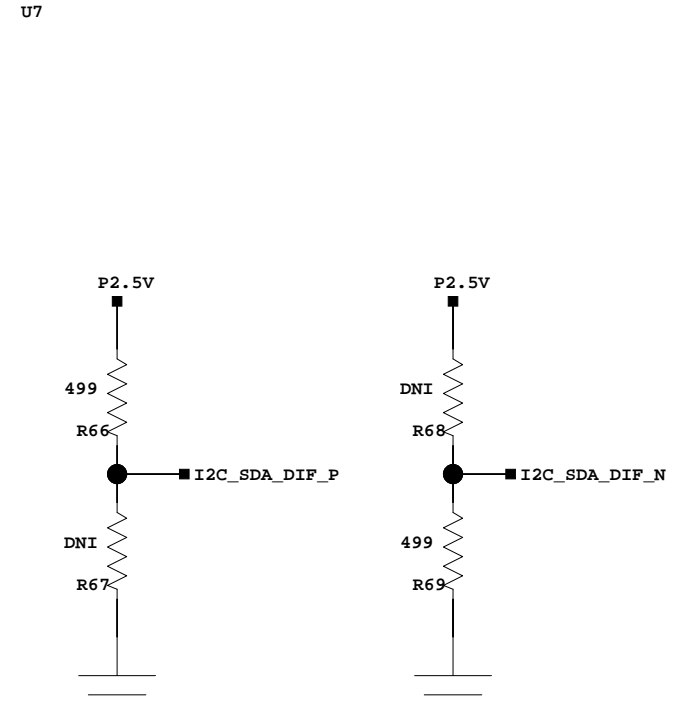
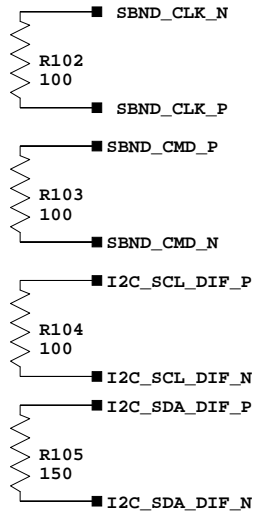
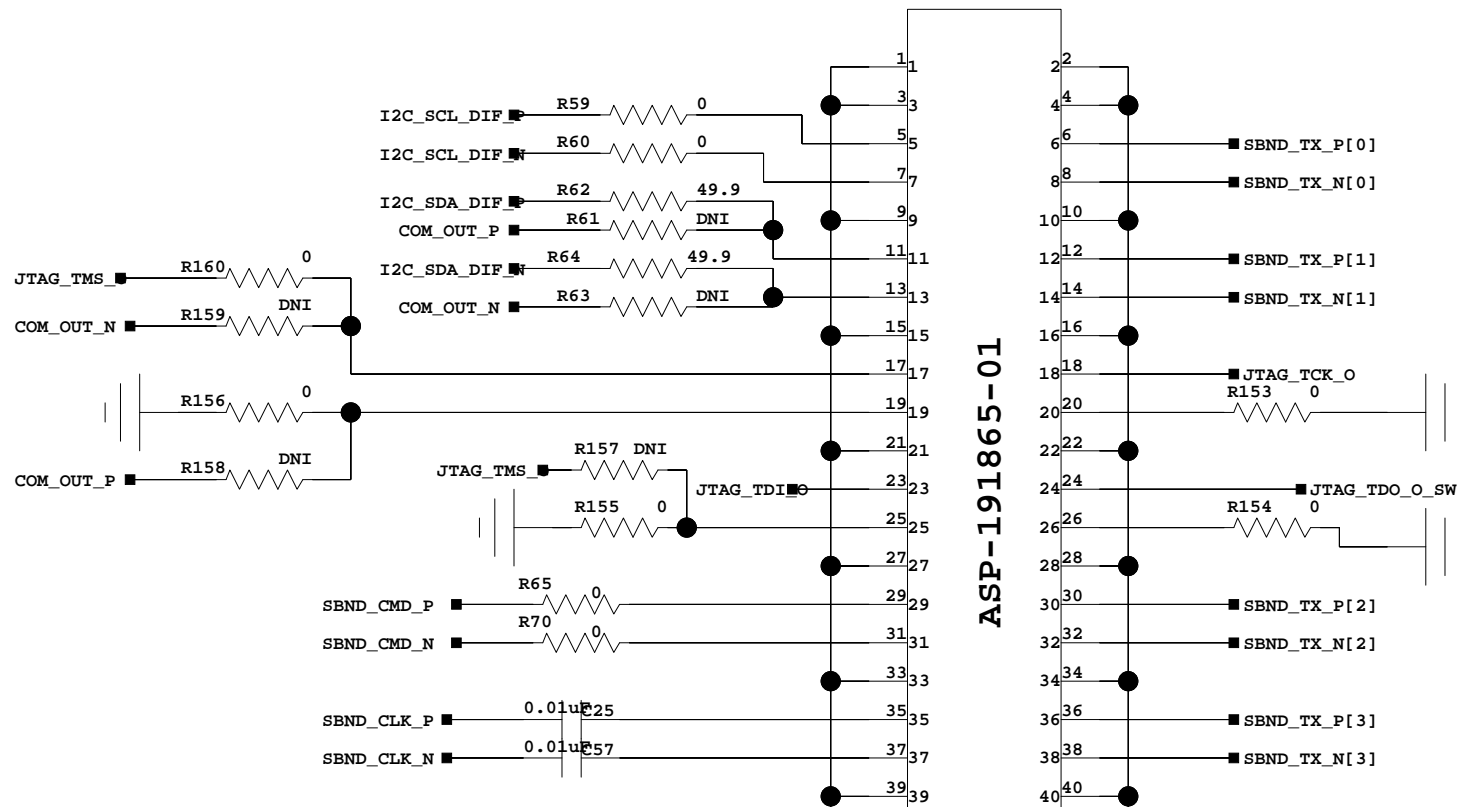
### DUNE\_MISC\_IO

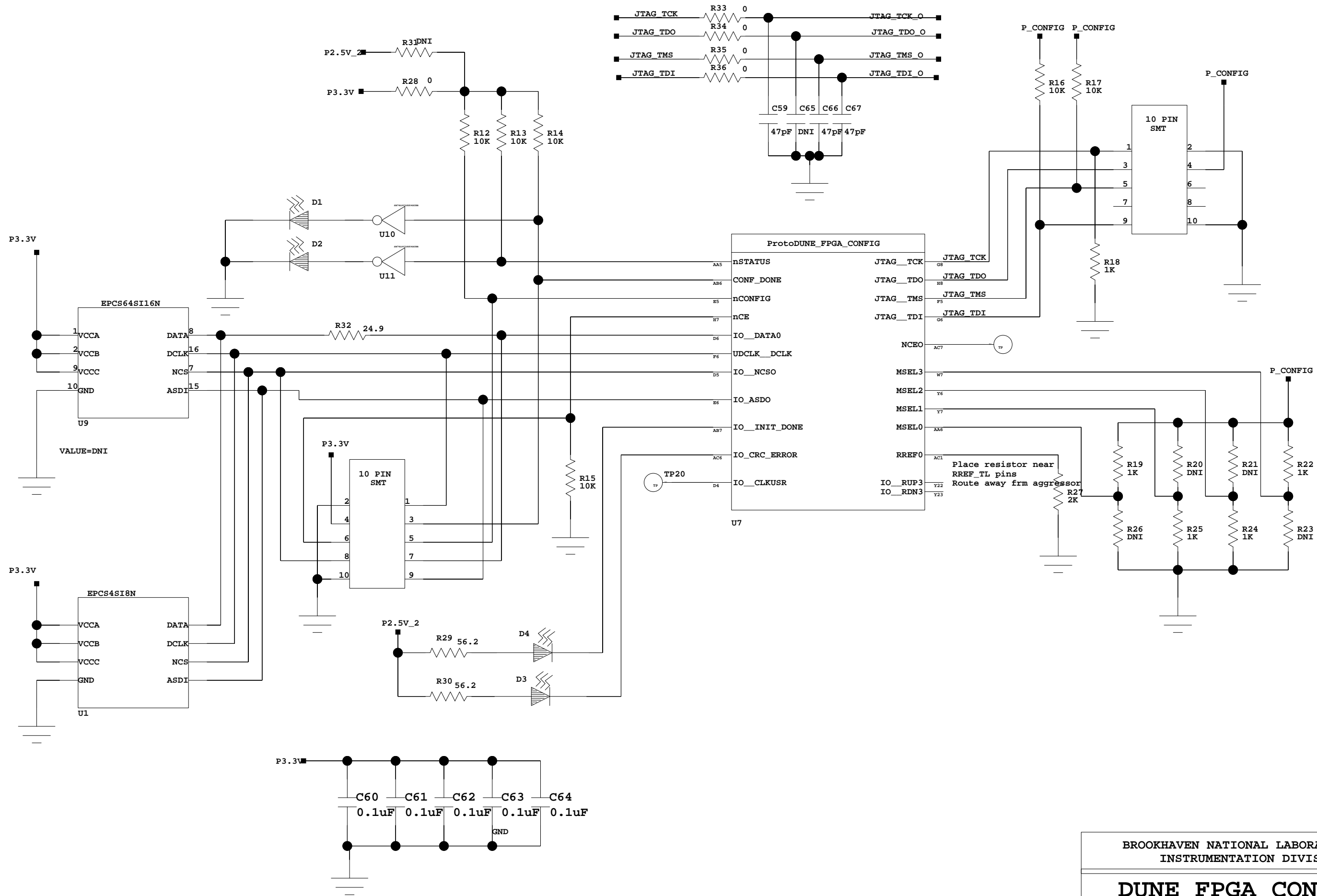
Date: 11/08/2017:10:38

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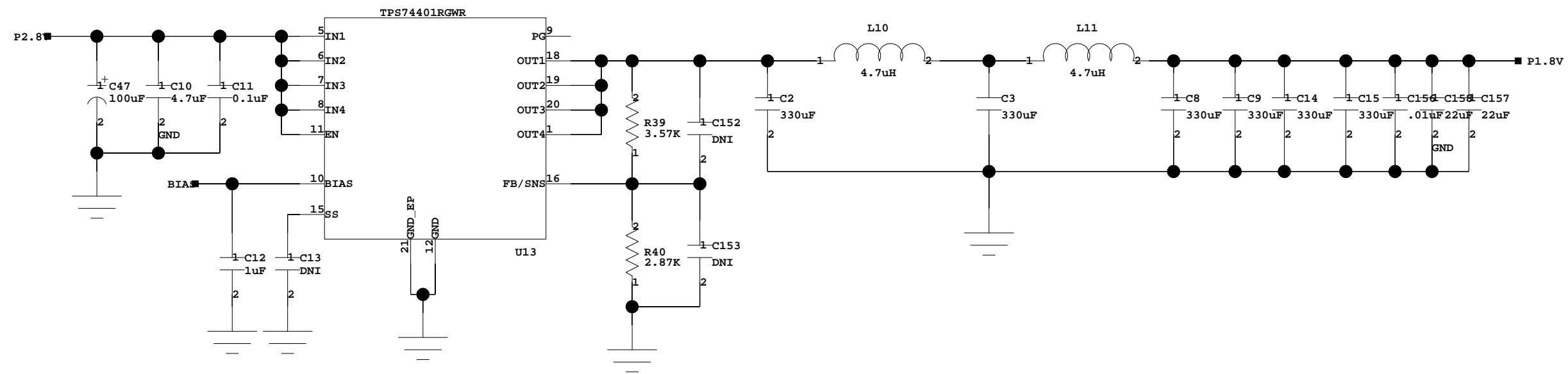
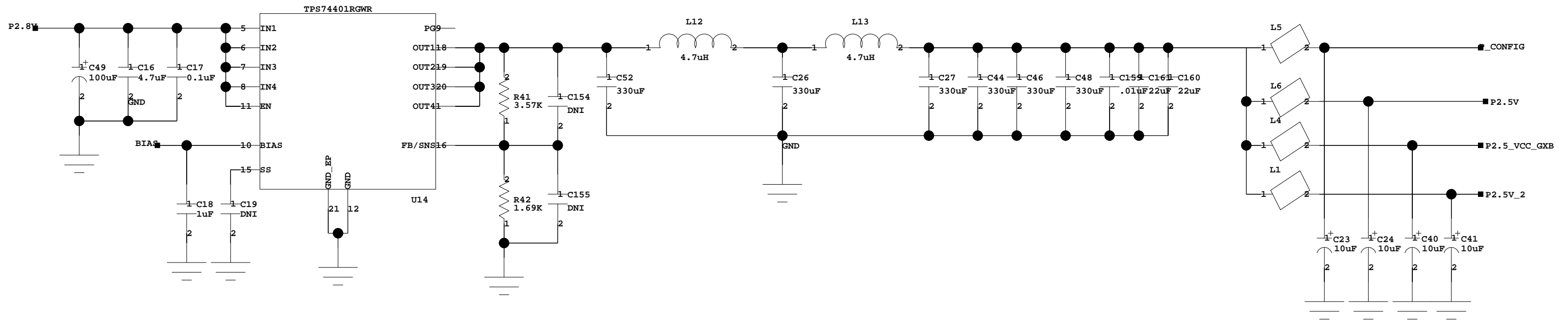


ProtoDUNE_FPGA_IO	
ProtoDUNE_TX_N[0]	Y3 SBND_TX_N[3]
ProtoDUNE_TX_P[0]	Y4 SBND_TX_P[3]
ProtoDUNE_TX_N[1]	V3 SBND_TX_N[2]
ProtoDUNE_TX_P[1]	V4 SBND_TX_P[2]
ProtoDUNE_TX_N[2]	T3 SBND_TX_N[1]
ProtoDUNE_TX_P[2]	T4 SBND_TX_P[1]
ProtoDUNE_TX_N[3]	F3 SBND_TX_N[0]
ProtoDUNE_TX_P[3]	F4 SBND_TX_P[0]
ProtoDUNE_CLK_N	AF14 SBND_CLK_N
ProtoDUNE_CLK_P	AF13 SBND_CLK_P
ProtoDUNE_CMD_N	AD14 SBND_CMD_N
ProtoDUNE_CMD_P	AC14 SBND_CMD_P
I2C_SCL_DIF_P	AF2 I2C_SCL_DIF_P
I2C_SCL_DIF_N	AF3 I2C_SCL_DIF_N
I2C_SDA_DIF_P	AE1 I2C_SDA_DIF_P
I2C_SDA_DIF_N	AE2 I2C_SDA_DIF_N
COM_OUT_N	J23 COM_OUT_N
COM_OUT_P	K23 COM_OUT_P
JTAG_SEL	D1 JTAG_SEL
ANALOG_SEL	C1 ANALOG_SEL







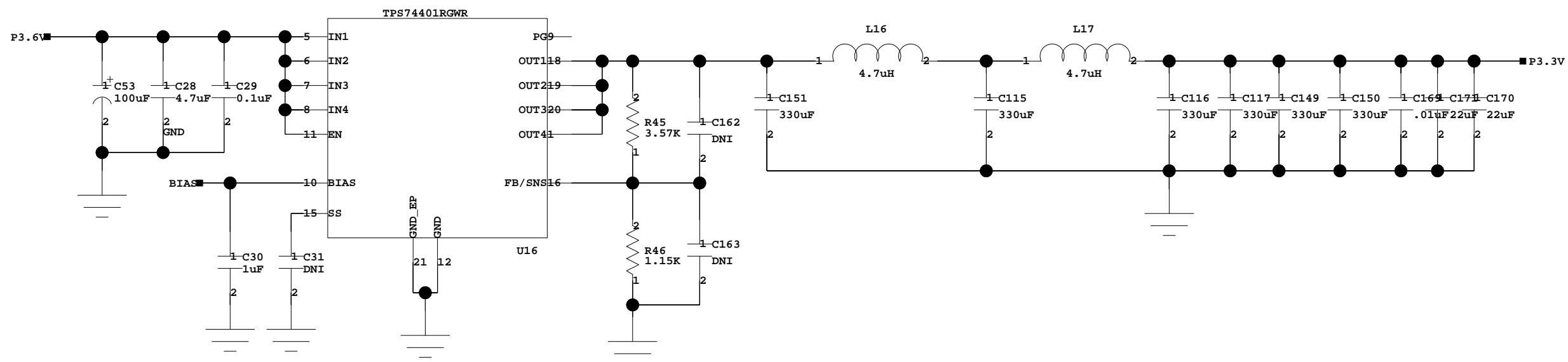
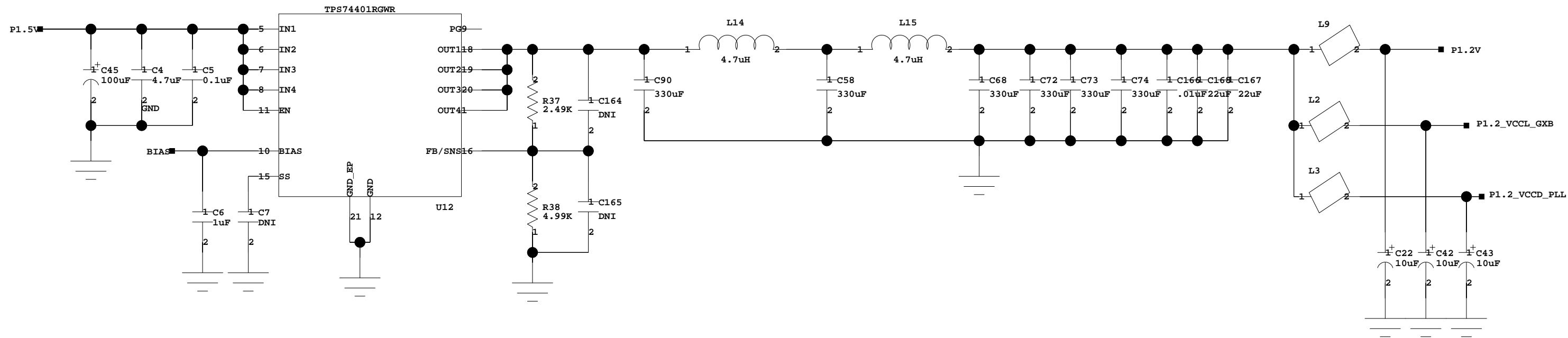


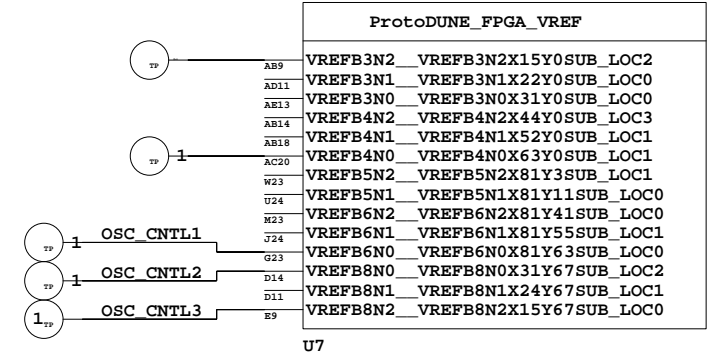
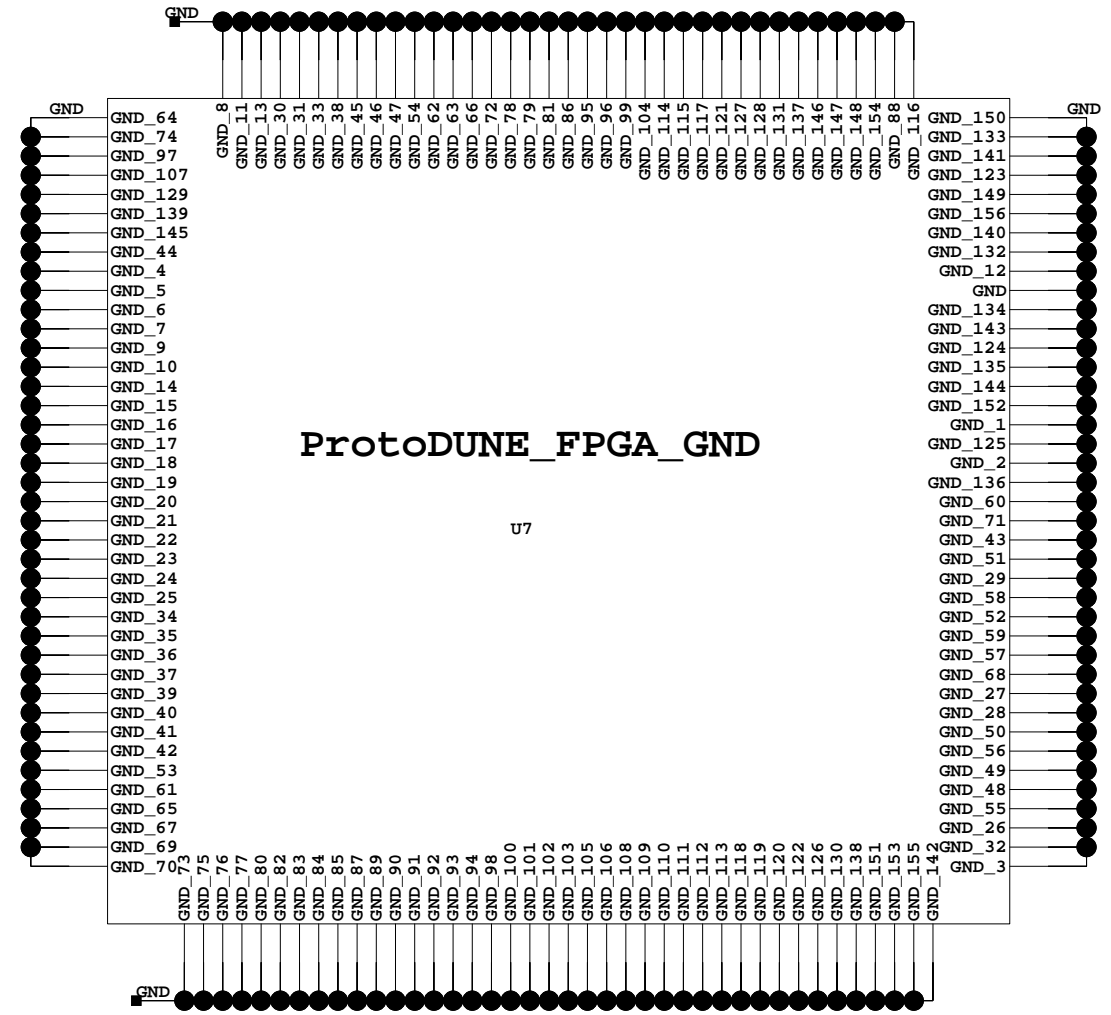
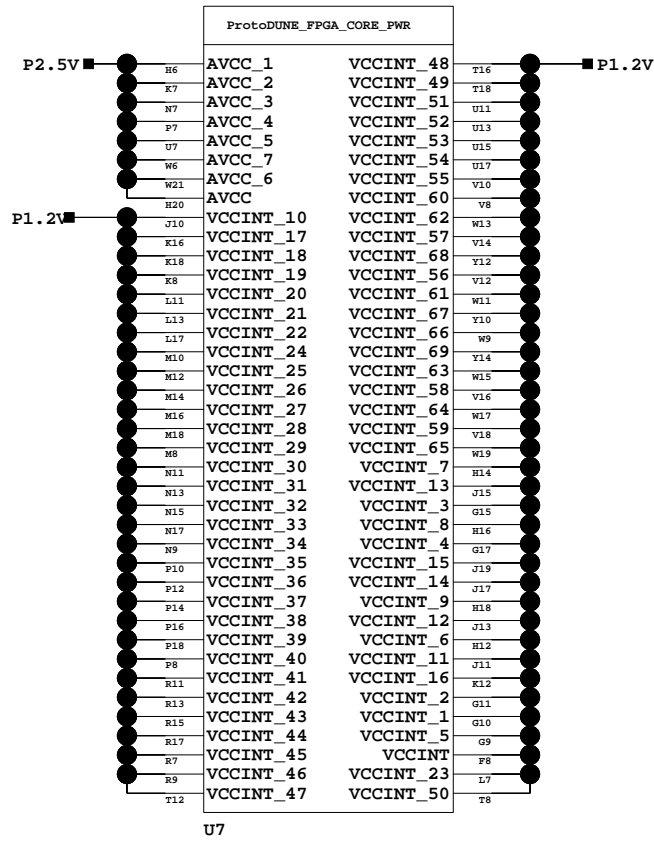
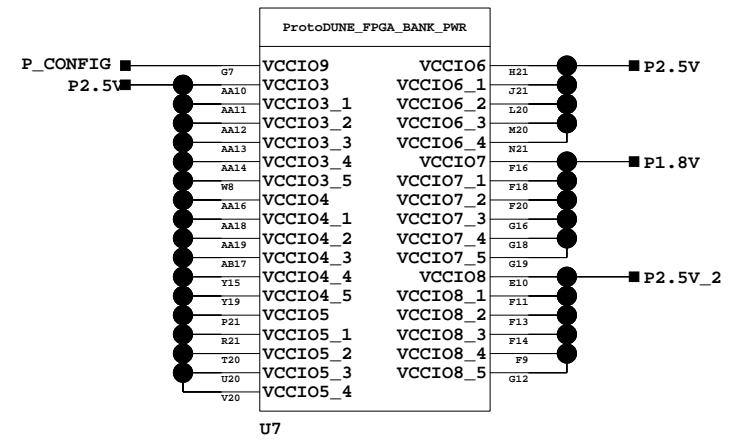
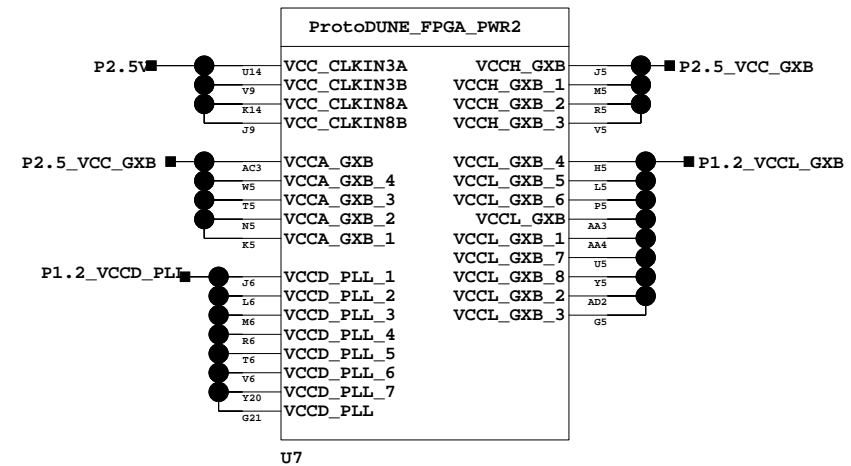
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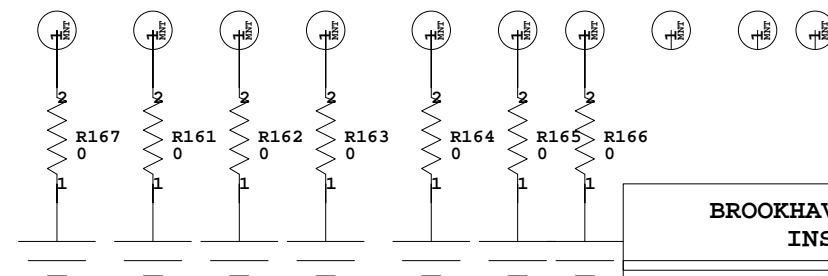
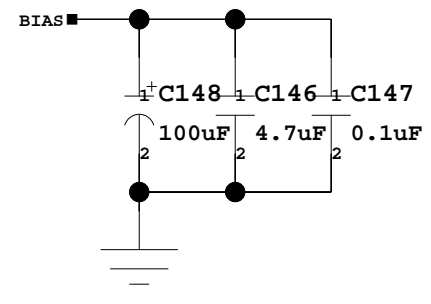
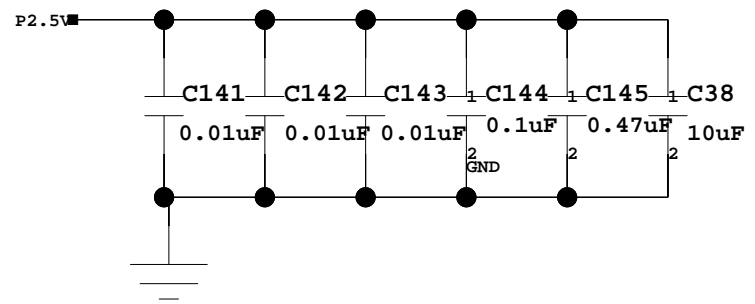
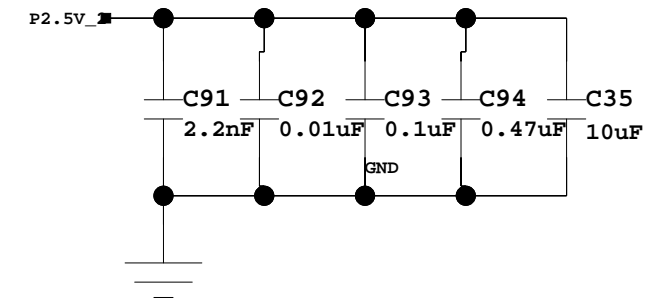
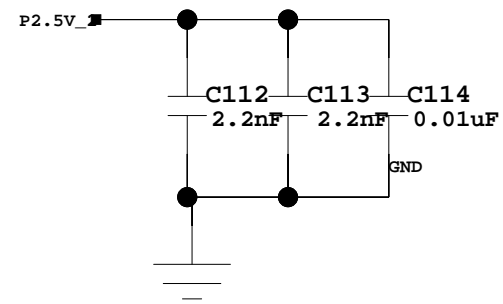
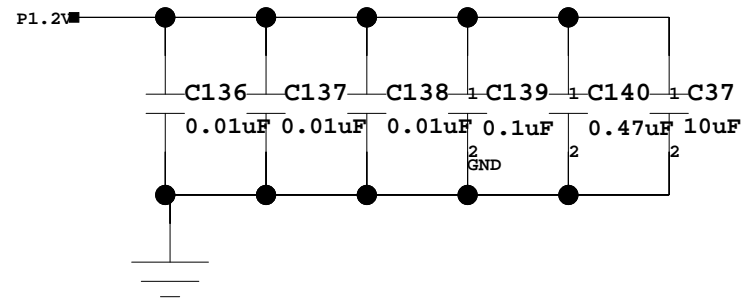
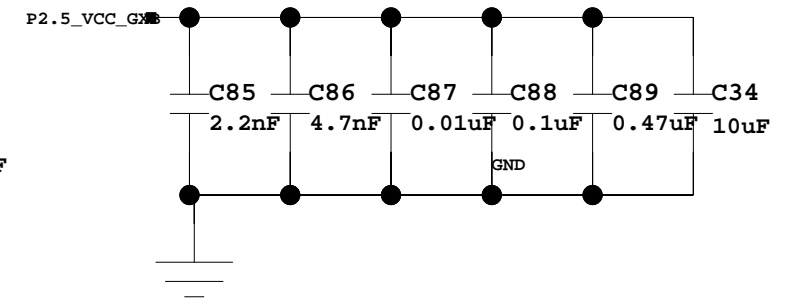
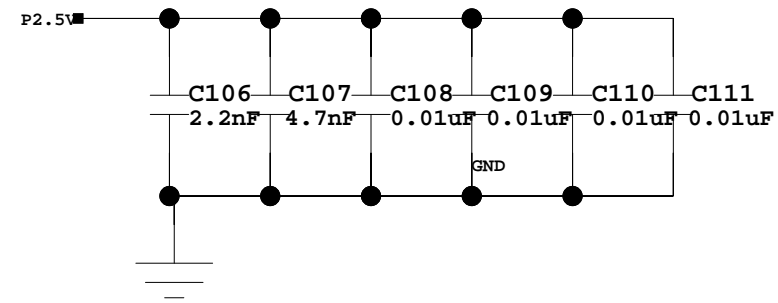
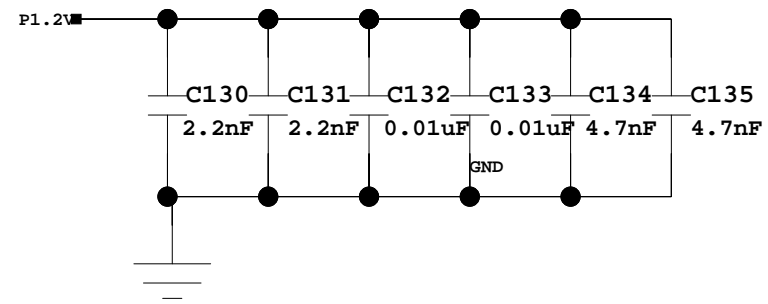
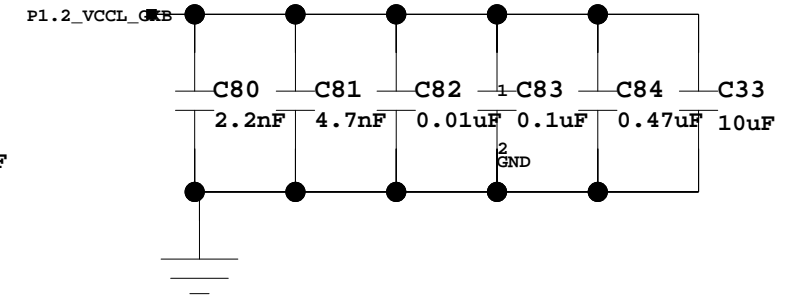
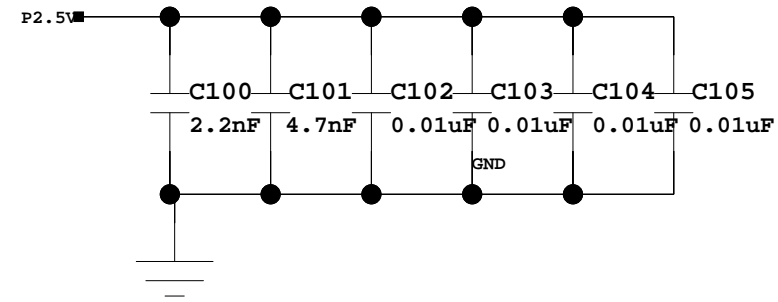
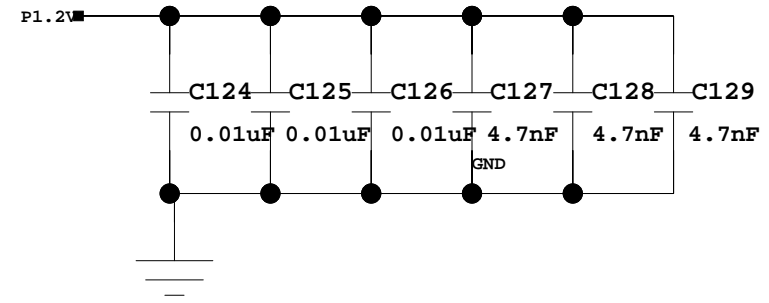
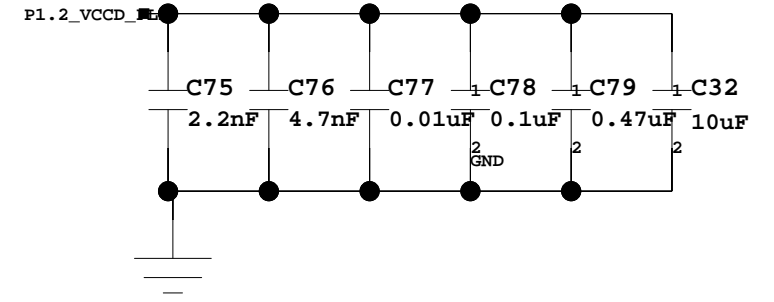
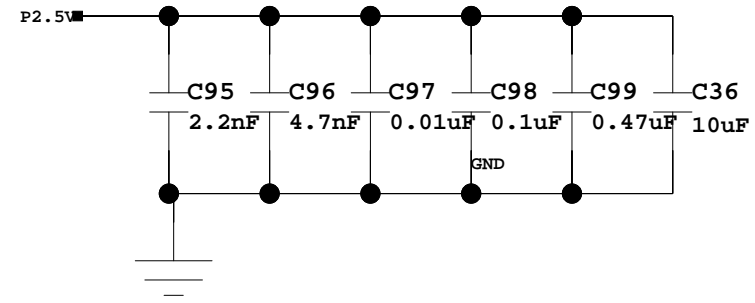
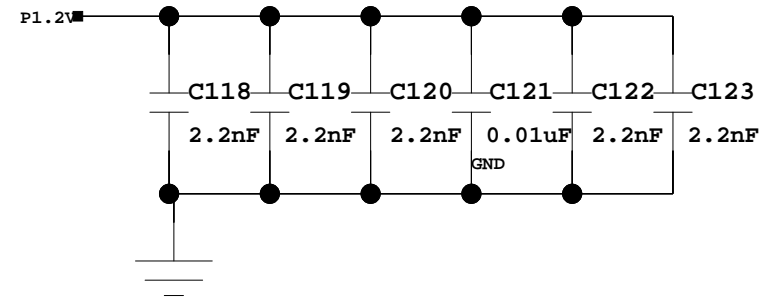
### DUNE\_PWR\_1

Date: 11/08/2017:10:52

DRAWN BY: Jack Fried







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# DUNE\_FPGA\_DECOUPLING

Date: 11/08/2017:10:38

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