SBND FEMB Mezzanine
Register Map Version 501

ADDRESS	NAME	R/W	BIT	Description
Basic Operations				
0x00	SYS_RESET	W	0	Set to reset entire system (AUTO clears)
0x00	REG_RESET	W	1	Set to reset system registers (AUOT clears)
0x00	TIME_STAMP_RESET	W	2	Set to time stamp reset, inherit from ProtoDUNE FM
0x00	ERROR_RST	W	3	reserved
0x00	/	/	31:4	reserved
0x01	ADC RESET	W	0	Set to reset ADC SPI interface logic (AUTO clears)
0x01	FE RESET	W	1	Set to reset FE ASICSPI (AUTO clears)
0x02	WRITE FE SPI	W	0	Set to write FE API (AUOT clears)
0x02	/	/	31:1	reserved
0x03	DATA_TEST Pattern	R/W	27:16	12bit test pattern to insert into data stream, 0x123 (default)
0x04	ADC CS POSITION	R/W	1:0	Bit 1 is not used actually. 0b00 (default)
0x05	TEST PULSE Amplitude	R/W	5:0	6-bit FPGA-DAC
0x05	Test Pulse Delay	R/W	15:8	Controls test pulse sample shift by 10ns/step Dealy = 10ns * N
0x05	Test Pulse Period	R/W	31:16	Set to control test pulse period 0x0000 (default). (dependent on ADC Sample Rate, 2MSPS default) T = Sample Period (500ns) * N 2MSPS: 00 = 500ns, 01=1us, 02=1.5us, …
0x06	/	/	/	reserved
0x07	/	/	/	reserved
0x08	ADC DISABLE REG (Data Stream Enable)	R/W	4	**When set to 1 the ADC readout is enabled (default =1)**, there is data stream to WIB. When set to 0 the readout is disabled, the data stream to WIB is prohibited.
0x08	FEMB System Clock Switch	R/W	16	Set to use onboard oscillator instead of system clock (Should ONLY be used for testing FEMB) 0(default), 1(onboard OSC)

ADDRESS	NAME	R/W	BIT	Description
0x08	FEMB System Clock Status	R	31:29	BIT29: clkbad1 indicator 0 = clock good 1 = clock bad BIT30: clkbad0 indicator 0 = clock good 1 = clock bad BIT31: active clock indicator 0 = clock 0 active 1 = clock 1 active
0x09	Stream_EN	R/W	0	Set to enable high-speed data If set to zero, high speed link will only see K codes **(Set to 1 for normal operation)**
0x09	PRBS_EN	R/W	1	Set to send PRBS test pattern PRBS: pseudorandom binary sequence 0 (default)
0x09	CNT_EN	R/W	2	Set to send test counter, 0(default)
0x09	ADC_DATA_EN	R/W	3	Set to send ADC data (must be set for normal operation)
0x0E (14)	/	/	/	reserved
0x0F (15)	/	/	/	reserved
0x10 (16)	FPGA_TP_EN	R/W	0	Set to enable FPGA-DAC calibration
0x10 (16)	ASIC_TP_EN	R/W	1	Set to enable ASIC-DAC calibration
0x10 (16)	DAC_SELECT	R/W	8	Select analog pulse source going to FE-ASIC 0 = FPGA-DAC on FM 1 = Analog pulse from the WIB
0x10 (16)	Analog Signal Selection	R/W	9	unused
0x10 (16)	Analog/JTAG Selection	R/W	10	Set to select analog monitor to be driven over JTAG TDO line
0x11 (17)	/	/	/	reserved
0x12 (18)	INT_TP_EN	R/W	0	Set to enable internal pulse generator (Period set by register 0x05) **0: enable, 1: disable**
0x12 (18)	EXT_TP_EN	R/W	1	Set to allow test pulse to be received by external timing control interface (register 0x05 delay&amplitude can be used) **0: enable, 1: disable**

ADDRESS	NAME	R/W	BIT	Description
0x13 (19)	FEMB_TST_MODE	R/W	0	Set to enable data test mode (ADC data is replaced with data stored in FEMB memory location (0x300-0x3ff))
0x14 (20)	TX_PLL_RESET	R/W	0	Set to reset FPGA transceiver PLL
0x14 (20)	TX_DIGITAL_RST	R/W	1	Set to reset FPGA transceiver digital logic
0x14 (20)	/	R/W	31:16	Not used. 0x01f8 (default)
0x15 (21)	ADC_PHASE_FE1	R/W	31:0	4 phase selections for FPGA to sample SDOs of ADCs for FE1, 0x00000000 (default)
0x16 (22)	ADC_PHASE_FE2	R/W	31:0	4 phase selections for FPGA to sample SDOs of ADCs for FE2, 0x00000000 (default)
0x17 (23)	ADC_PHASE_FE3	R/W	31:0	4 phase selections for FPGA to sample SDOs of ADCs for FE3, 0x00000000 (default)
0x18 (24)	ADC_PHASE_FE4	R/W	31:0	4 phase selections for FPGA to sample SDOs of ADCs for FE4, 0x00000000 (default)
0x19 (25)	ADC_PHASE_FE5	R/W	31:0	4 phase selections for FPGA to sample SDOs of ADCs for FE5, 0x00000000 (default)
0x1A (26)	ADC_PHASE_FE6	R/W	31:0	4 phase selections for FPGA to sample SDOs of ADCs for FE6, 0x00000000 (default)
0x1B (27)	ADC_PHASE_FE7	R/W	31:0	4 phase selections for FPGA to sample SDOs of ADCs for FE7, 0x00000000 (default)
0x1C (28)	ADC_PHASE_FE8	R/W	31:0	4 phase selections for FPGA to sample SDOs of ADCs for FE8, 0x00000000 (default)
0x1D (29)	ADC_DLY_FE1	R/W	31:0	Bit shifts for ADC data of FE1, 0x00000000 (default)
0x1E (30)	ADC_DLY_FE2	R/W	31:0	Bit shifts for ADC data of FE2, 0x00000000 (default)
0x1F (31)	ADC_DLY_FE3	R/W	31:0	Bit shifts for ADC data of FE3, 0x00000000 (default)
0x20 (32)	ADC_DLY_FE4	R/W	31:0	Bit shifts for ADC data of FE4, 0x00000000 (default)
0x21 (33)	ADC_DLY_FE5	R/W	31:0	Bit shifts for ADC data of FE5, 0x00000000 (default)
0x22 (34)	ADC_DLY_FE6	R/W	31:0	Bit shifts for ADC data of FE6, 0x00000000 (default)
0x23 (35)	ADC_DLY_FE7	R/W	31:0	Bit shifts for ADC data of FE7, 0x00000000 (default)
0x24 (36)	ADC_DLY_FE8	R/W	31:0	Bit shifts for ADC data of FE8, 0x00000000 (default)

ADDRESS	NAME	R/W	BIT	Description
0x29 (41)	ADC_SYNC_Mode	R/W	1:0	ADC sampling clock synchronization select 00 = Normal -- Sync convert signal to 200MHz clk, default 01 = Free running -- No synchronization 10 = follow -- System convert signal passed to ADC with no synchronization to system clock 11 = Convert clock disabled
0x2A (42)	FEMB_TST_SEL	R/W	3:0	Test mode (Fake data Generator) 0 = Normal Mode (Real Data) 1 = Test Pattern loaded to all channels (data value of REG 0x03) 2 = Waveform data generator data loaded in memory location (0x300 -0x3FF) 3 = Channel indicator 0xA, B, C Where A = FEM NUMBER (REG 42(7:0)) B = Chip number C = Channel number 4 = sawtooth waveform
0x2A (42)	FEMB_NUMBER	R/W	7:4	Used with FEMB_TST_SEL mode 3
0x2B (43)	TEST_PULSE_WIDTH	R/W	15:0	Test pulse width control. (Default 0xA00) 0 = 10ns 1 = 20ns 2 = 30ns
FE ASIC SPI Reg Data				
0x200-0x248	ASIC SPI WRITE DATA	R/W	31:0	ASIC SPI data to be written into the ASICs
0x250-0x298	ASIC SPI READBACK	R/W	31:0	ASIC SPI data to be read back
WFM_GEN_DATA				
0x300-0x3FF	WFM_GEN_DATA	R/W	23:0	256 samples of TEST pattern memory for fake data generator (must set registers 3 bits 7..0 and must set register 19 Bits (11..0) = odd channels Bits(23..12) = even channels
EPCS memory W/R				

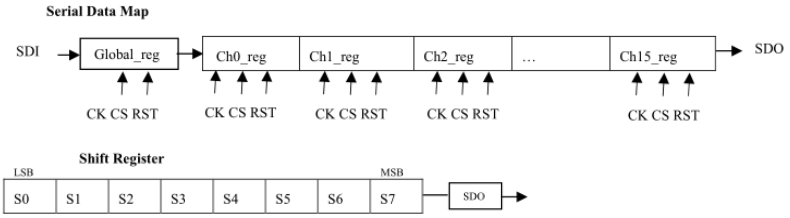
ADDRESS	NAME	R/W	BIT	Description
0x0A (10)	*FPGA_F_OP_CODE*	*R/W*	*7:0*	*Set this to the proper FLASH OP-CODE* *OP_CODES 0x00 (default)* *0x02 = Write memory – write enable must be set* *0x03 = Read memory* *0x04 = Disable Write Enable* *0x05 = Read status* *0x06=Write Enable (use before write @ bulk erase)* *0xAB = Read Silicon ID (result is stored in status reg)* *0xC7 = Erase bulk (write enable must be set)*
0x0A (10)	*FPGA_F_STRT_OP*	*R/W*	*8*	*Set this bit to start FPGA FLASH operation (user must clear) (FLASH) 0x0 (default)*
0x0B (11)	*FPGA_F_ADDR*	*R/W*	*23:0*	*Set for start address of the Flash 256 byte operation (FLASH) 0x0 (default)*
0x0C (12)	*FPGA_F_status*	*R*	*31:0*	*FPGA_F_Status*
0x0D (13)	*FPGA_F_ENABLE*	*R/W*	*0*	*Set to enable Flash programmer*
0x200-0x208	*FPGA_F_WR MEMORY*	R/W	31:0	*Storage for Writing FPGA EPCS 256 bytes 0x0 (default)*
0x240-0x248	*FPGA_F_RD MEMORY*	R/W	31:0	*Storage for read back of FPGA EPCS 256 bytes 0x0 (default)*
Firmware Status				
0x100 (256)	SCRATCH_PAD	R	31:0	Register scratch pad 0x0 (default)
0x101 (257)	VERSION ID	R	15:0	FIRMWARE VERSION ID
0x101 (257)	BOARD ID	R	31:16	Board ID read form dip switch
0x102 (258)	COMPILED VERSION	R	31:0	Complied version number (auto increments)
0x103 (259)	DATE COMPILED	R	31:0	Date Complied (in HEX)
0x104 (260)	TIME COMPILED	R	31	Time Complied (in HEX)

Basic Operation for General Users

1. FE ASICs Configuration

a. FE ASIC reg map

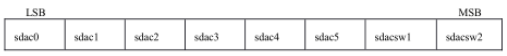
According to LARASIC7 datasheet, each FE-ASIC has a 144-bit shift register.



Data is shifted into the load shift register on the rising edge of CK while CS is high.
The MSB is shifted into position D0 on the first rising edge of CK.
The LSB is shifted into position D0 on the 8th rising edge of CK.
The MSB is shifted out of SDO on the 9th rising edge of CK.
The LSB is shifted out of SDO on the 16th rising edge of CK.

NOTE: The default value of each register is 00.

RES - Reserved.



SLKH - Leakage current increase x10, 0 = disabled, 1 = enabled
STB - 0 = Monitor analog channel signal. 1 = Monitor temperature or bandgap reference.
STB1 - 0 = Monitor temperature. 1 = Monitor bandgap reference.
SLK - Leakage current control. 0 = 500 pA. 1 = 100 pA.
S16 - Enable high filter in ch16, 0 = disabled, 1 = enabled
SDC - Output coupling. 0 = dc coupling. 1 = ac coupling.

STS - Test capacitance. 0 = disabled. 1 = enabled.
SNC - Baseline selection. 0 = 900 mV (for non-collecting mode). 1 = 200 mV (for collecting mode).
SG (0,1) - Gain selection. 00 = 4.7 mV/fC, 10 = 7.8 mV/fC, 01 = 14 mV/fC, 11 = 25 mV/fC.
ST (0,1) - Peak time selection. 00 = 1.0 us, 10 = 0.5 us, 01 = 3 us, 11 = 2 us.
SBF - Output buffer bypass. 0 = output buffer powered down and bypassed. 1 = output buffer selected.
SMN - Output monitor enable. 0 = monitor disabled. 1 = monitor enabled: channel output routed to Test pad (after sdac switch) - Do not use with SDACSW1 and/or SDACSW2 high. Do not enable more than one monitor at a time.

Conflict configurations:
1. SMN+SW1 = will short the channel output with the injection input
2. SMN+SW1+SW2 = will short the channel output with the DAC output

Let's assume each FE is configured with Gain 7.8mV/fC, Shaping time 2.0us, Baseline 900mV, 500pA Leakage current, Calibration disable, FE DC mode, Buffer on, and monitor off.

b. FPGA Registers map to FE registers

FPGA register addresses from 0x200 to 0x248 are reserved for AM ASICs configuration. For SBND AM, FPGA register addresses from 0x200 to 0x223 are used to configure 8 FE ASICs (144bits*8 = 1152bits = 36bytes = 9*32 bytes). The mapping relation is shown in figure below.

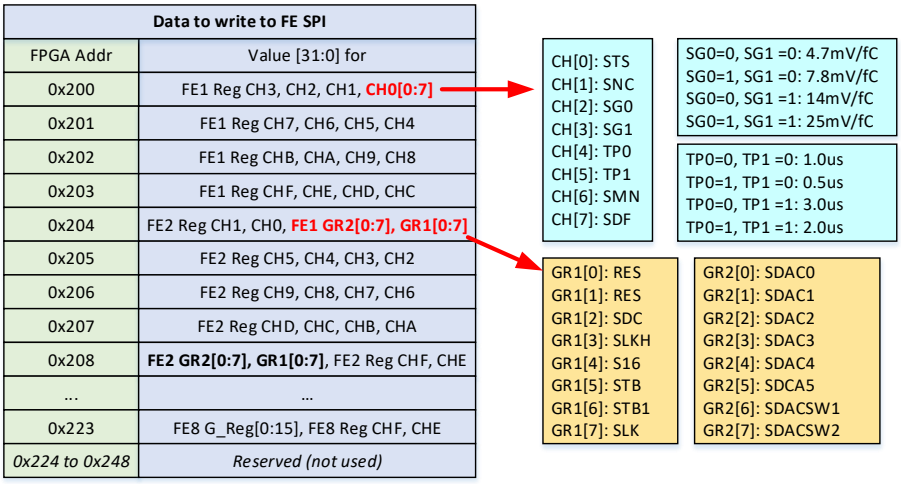


Figure 1 SPI data to write to FEs

Similarly, FPGA register addresses from 0x250 to 0x298 are reserved to save SPI data read back from AM ASICs. For SBND AM, FPGA register addresses from 0x250 to 0x273 are used to save SPI data from 8 FE ASICs (144bits*8 = 1152bits = 36bytes = 9*32 bytes). The mapping relation is shown in figure below.

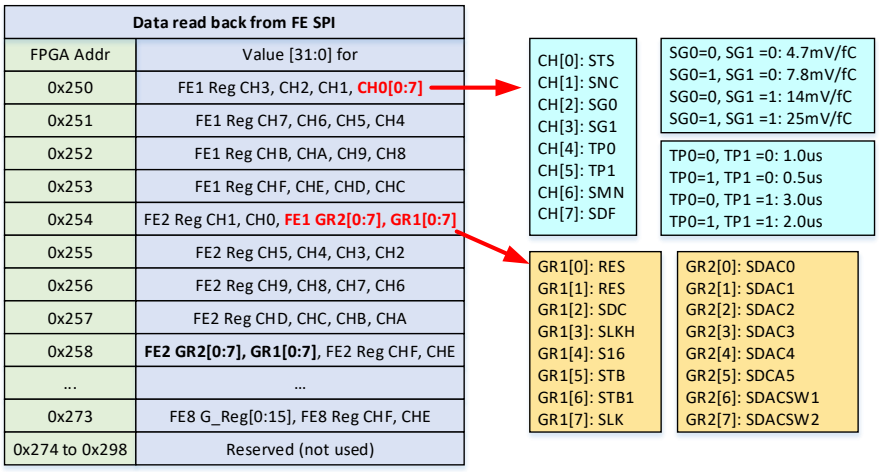


Figure 2 SPI data read back from Fes

c. Class FE_REG_MAPPING in fe_reg_mapping.py

Class FE_REG_MAPPING is designed to configure 8 FEs on a AM. The priority order is set_fe_board() > set_fechip() > set_fechn_reg() or set_fechip_global(). The higher priority function overwrites the data from the lower priority function.

2. Experiment mode configuration

a. WIB and FEMB available scanning

First, we should scan the available WIBs mounted to switch. Then we should check the available FEMBs mounted on each WIB.

Initial checkout helps verify all links are functional. It should include

b. Initial checkout

Initial checkout helps verify all links are functional. It should include

(i) WIB version checkout, which proves UDP link between WIB and Host-PC is good or not

(ii) FEMB version checkout, which proves I2C link between WIB and FEMB is good or not

(iii) LINK_STAT & EQ_STAT checkout, which proves high speed links (4*1.28Gbps) between WIB and FEMB are good or not

Initial checkout should be treated as exception process. It should be finished to scan all WIBs and FEMbs in operation. So, any inactive WIB or inactive FEMB should be masked to avoid further operations on these WIBs or FEMBs.

c. FE ASIC configuration

d. FEMB configuration

e. WIB configuration

Advanced operations for experts

1. Program fixed information to Flash

FEMB number (including AM & FM), APA number, Location Number and other information can be programmed into Flash memory, which won't be erased after power cycle.

2. Update FW through UDP

3. FM QC test Procedure

a. FM programming

S1: In order to test JTAG interface, program FPGA with USB Blaster II through JTAG test board and 7 m mini-SAS cable.

PASS → JTAG interface is Good

S2: Program FLASH memory with *.rpd file through JTAG test board and 7m mini-SAS cable.

PASS → Done

b. FM testing

SBND Warm Interface Board (WIB)
Register Map Version 117

ADDRESS	NAME	R/W	BIT	Description
0x00	GLB_i_RESET	W	0	Global reset, auto clears
0x00	REG_RESET	W	1	Register reset, auto clears
0x00	UDP_RESET	W	2	UDP interface reset, auto clears
0x00	ALG_RESET	W	3	SBND PWM CLK Encoder reset, auto clears
0x00	HSD_RESET	W	4	FEMB highspeed receivers reset, auto clears
0x01	SBND_CAL	R/W	0	Encode a calibration pulse in 2MHz sample clock by duty cycle. The calibration pulse is sent to 4 FEMBs of a WIB at the same time. Set to 1: a calibration pulse command is encoded in 2MHz sample clock. **It doesn't automatically clear, MUST be set to 0** through UDP before generating another calibration pulse command The priority order: bit0 > bit1 > bit2 > bit3. It is recommended to set any bit exclusively among bit0-3
0x01	SBND_TS_RST	R/W	1	Time Stamp Reset Command encoded in 2MHz sample clock (PWM, duty cycle). Setting this bit to 1 resets and synchronizes time stamp counter of FEMBs on a WIB. All FEMBs on a WIB will have same time stamp counter number for the sampling event. **It doesn't automatically clear, MUST be set to 0** through UDP before generating another command The priority order: bit0 > bit1 > bit2 > bit3. It is recommended to set any bit exclusively among bit0-3

ADDRESS	NAME	R/W	BIT	Description
0x01	SBND_STOP_DAQ	R/W	2	Encoded command in 2MHz PWM sample clock that forces FEMB to stop sending data to WIB. Set the bit to 1, all FEMBs on the same WIB stop sending data to WIB. **It doesn't automatically clear, MUST be set to 0** through UDP before generating another command. The priority order: bit0 > bit1 > bit2 > bit3. It is recommended to set any bit exclusively among bit0-3
0x01	SBND_START_DAQ	R/W	3	Encoded command in 2MHz PWM sample clock that forces FEMB to start sending data to WIB. Set the bit to 1, all FEMBs on the same WIB start sending data to WIB. **It doesn't automatically clear, MUST be set to 0** through UDP before generating another command. The priority order: bit0 > bit1 > bit2 > bit3. It is recommended to set any bit exclusively among bit0-3
0x02	WIB_LED [1:0]	R/W	1:0	Control 2 LEDs on front panel
0x03	-NOT USED-	/	/	Reserved
0x04	FEMB_CLK_SEL	R/W	0	Set to 0: select system clock (100MHz) from WIB FPGA (default) Set to 1: select system clock from SI5344
0x04	FEMB_CMD_SEL	R/W	1	Set to 0: select system CMD clock (2MHz) from WIB FPGA (default) Set to 1: select system CMD clock (2MHz) from PTC (MBB → PTC → PTB → WIB → FEMB)
0x04	FEMB_INT_CLK_SEL	R/W	3:2	2b00 (default) and 2b01: select SBND_CLK from SI5344 2b10: select clk_100MHz from PLL driven by a onboard 50MHz OSC (bypass SI5344)

ADDRESS	NAME	R/W	BIT	Description
0x05	PWR_MES_SEL	R/W	7:0	Set to choose WIB monitoring parameters from LTC2991CMS 0x00: BIAS_VCC and BIAS_TEMP 0x01: BRD1_VCC and BRD1_TEMP 0x02: BRD1_V1 and BRD1_C1 0x03: BRD1_V2 and BRD1_C2 0x04: BRD1_V3 and BRD1_C3 0x05: BRD1_V4 and BRD1_C4 0x06: BRD1_V5 and BRD1_C5 0x07: BRD2_VCC and BRD2_TEMP 0x08: BRD2_V1 and BRD2_C1 0x09: BRD2_V2 and BRD2_C2 0x0A: BRD2_V3 and BRD2_C3 0x0B: BRD2_V4 and BRD2_C4 0x0C: BRD2_V5 and BRD2_C5 0x0D: BRD3_VCC and BRD3_TEMP 0x0E: BRD3_V1 and BRD3_C1 0x0F: BRD3_V2 and BRD3_C2 0x10: BRD3_V3 and BRD3_C3 0x11: BRD3_V4 and BRD3_C4 0x12: BRD3_V5 and BRD3_C5 0x13: BRD4_VCC and BRD4_TEMP 0x14: BRD4_V1 and BRD4_C1 0x15: BRD4_V2 and BRD4_C2 0x16: BRD4_V3 and BRD4_C3 0x17: BRD4_V4 and BRD4_C4 0x18: BRD4_V5 and BRD4_C5 0x19: WIB_VCC and WIB_TEMP 0x1A: WIB_V1 and WIB_C1 0x1B: WIB_V2 and WIB_C2 0x1C: WIB_V3 and WIB_C3 0x1D: WIB_V4 and WIB_C4 0x1E: FE_VCC and FE_TEMP 0x1F: BRD1_V6 and BRD1_C6 0x20: BRD2_V6 and BRD2_C6 0x21: BRD3_V6 and BRD3_C6 0x22: BRD4_V6 and BRD4_C6 Other: “DEADBEEF”
0x05	PWR_MES_start	R/W	16	1: enable LTC2991CMS conversion operation 0(default): disable LTC2991CMS conversion operation
0x05	FILTER_EN	R/W	17	0 (default): disable LTC2991CMS digital filter 1: enable LTC2991CMS digital filter
0x06	PWR_MES_OUT	R	31:0	Read back WIB monitoring parameters required by command 0x05
0x07	CHN_SEL	R/W	3:0	Set to select FE CHN# (0~15)
0x07	CHN_SEL	R/W	11:8	Set to select FE# (0~7)
0x07	BRD_SEL	R/W	19:16	Set to select FEMB# (0~3)

ADDRESS	NAME	R/W	BIT	Description
0x07	UDP_DISABLE	R/W	31	0(default): enable high-speed data stream, data of a FE chip (16 chns) 1: disable high-speed data stream
0x08	PWR_EN_3_6V_BRD0	R/W	0	ON (1) / OFF (0) DC/DC **3.9V** for BRD0 FM
0x08	PWR_EN_2_8V_BRD0	R/W	1	ON (1) / OFF (0) DC/DC **3.0V** for BRD0 FM
0x08	PWR_EN_2_5V_BRD0	R/W	2	ON (1) / OFF (0) DC/DC **3.3V** for BRD0 AM
0x08	PWR_EN_1_5V_BRD0	R/W	3	ON (1) / OFF (0) DC/DC **1.8V** for BRD0 FM
0x08	PWR_EN_BIAS_BRD0	R/W	16	ON (1) / OFF (0) LDO bias for BRD0
0x08	PWR_EN_2_5V_FE_BRD0	R/W	21	ON (1) / OFF (0) LDO **2.8V FE** for BRD0 AM
0x08	PWR_EN_3_6V_BRD1	R/W	4	ON (1) / OFF (0) DC/DC **3.9V** for BRD1 FM
0x08	PWR_EN_2_8V_BRD1	R/W	5	ON (1) / OFF (0) DC/DC **3.0V** for BRD1 FM
0x08	PWR_EN_2_5V_BRD1	R/W	6	ON (1) / OFF (0) DC/DC **3.3V** for BRD1 AM
0x08	PWR_EN_1_5V_BRD1	R/W	7	ON (1) / OFF (0) DC/DC **1.8V** for BRD1 FM
0x08	PWR_EN_BIAS_BRD1	R/W	17	ON (1) / OFF (0) LDO bias for BRD1
0x08	PWR_EN_2_5V_FE_BRD1	R/W	22	ON (1) / OFF (0) LDO **2.8V FE** for BRD1 AM
0x08	PWR_EN_3_6V_BRD2	R/W	8	ON (1) / OFF (0) DC/DC **3.9V** for BRD2 FM
0x08	PWR_EN_2_8V_BRD2	R/W	9	ON (1) / OFF (0) DC/DC **3.0V** for BRD2 FM
0x08	PWR_EN_2_5V_BRD2	R/W	10	ON (1) / OFF (0) DC/DC **3.3V** for BRD2 AM
0x08	PWR_EN_1_5V_BRD2	R/W	11	ON (1) / OFF (0) DC/DC **1.8V** for BRD2 FM
0x08	PWR_EN_BIAS_BRD2	R/W	18	ON (1) / OFF (0) LDO bias for BRD2
0x08	PWR_EN_2_5V_FE_BRD2	R/W	23	ON (1) / OFF (0) LDO **2.8V FE** for BRD2 AM
0x08	PWR_EN_3_6V_BRD3	R/W	12	ON (1) / OFF (0) DC/DC **3.9V** for BRD3 FM
0x08	PWR_EN_2_8V_BRD3	R/W	13	ON (1) / OFF (0) DC/DC **3.0V** for BRD3 FM
0x08	PWR_EN_2_5V_BRD3	R/W	14	ON (1) / OFF (0) DC/DC **3.3V** for BRD3 AM
0x08	PWR_EN_1_5V_BRD3	R/W	15	ON (1) / OFF (0) DC/DC **1.8V** for BRD3 FM
0x08	PWR_EN_BIAS_BRD3	R/W	19	ON (1) / OFF (0) LDO bias for BRD3
0x08	PWR_EN_2_5V_FE_BRD3	R/W	24	ON (1) / OFF (0) LDO **2.8V FE** for BRD3 AM
0x08	PWR_CLK_IN (1)	R/W	20	5V BIAS DC/DC enable
0x09	TST_WFM_GEN_MODE	R/W	7:4	0x0 (default): data from FEMB 0x1: sawtooth waveform generated from WIB 0x2: channel-mapping number = FEMB#N(0-3) * 256 + ASIC#M(0-7) * 16 + FE_chn#X(0-15)
0x0A (10)	I2C_WR_STRB	R/W	0	Set to start SI5344 I2C Write
0x0A (10)	I2C_WR_STRB	R/W	1	Set to start SI5344 I2C Read

ADDRESS	NAME	R/W	BIT	Description
0x0A (10)	SILABS_RST	R/W	8	0 (default): 1: set to hold the SI5344 in reset
0x0B (11)	I2C_NUM_BYTES	R/W	3:0	SI5344 I2C control -- Number of bytes to write
0x0B (11)	I2C_ADDRESS	R/W	15:8	SI5344 I2C control -- Address to be accessed
0x0B (11)	I2C_DIN	R/W	23:16	SI5344 I2C control -- I2C data being written
0x0C (12)	I2C_DOUT_S1	R	15:0	SI5344 I2C control --I2C data read back
0x0C (12)	SI5344_LOL	R	16	SI5344 PLL clock status -- 1 = locked
0x0C (12)	SI5344_LOSXAXB	R	17	SI5344 PLL clock status – 1 = locked
0x0C (12)	SI5344_INTR	R	18	SI5344 --- NOT USED
0x0C (12)	/	R	19	0
0x0C (12)	/	R	31:20	0x000
0x0D (13)	-NOT USED-	/	/	reserved
0x0E (14)	-NOT USED-	/	/	reserved
0x0F (15)	UDP_BURST_MODE	R/W	3:0	Bloomberg Mode (ask Jack) 0: normal operation 1: collection data 2: readout mode 3: clear fifo
0x0F (15)	UDP_BURST_EN	R/W	4	1: Set to enable burst mode (ask Jack)
0x10 (16)	UDP_SAMP_TO_SAVE	R/W	15:0	Set FIFO size for burst mode,
0x11 (17)	GXB_analogreset	R/W	0	GXB transceiver analog reset
0x11 (17)	GXB_digitalreset	R/W	1	GXB transceiver digital reset
0x11 (17)	RST_NEVIS_DAQ_LINK	R/W	4	Set to reset link to NEVIS DAQ

ADDRESS	NAME	R/W	BIT	Description
0x12 (18)	link_stat_sel	R/W	3:0	00: select the status of HS link0 of a FEMB0 01: select the status of HS link1 of a FEMB0 02: select the status of HS link2 of a FEMB0 03: select the status of HS link3 of a FEMB0 04: select the status of HS link0 of a FEMB1 05: select the status of HS link1 of a FEMB1 06: select the status of HS link2 of a FEMB1 07: select the status of HS link3 of a FEMB1 08: select the status of HS link0 of a FEMB2 09: select the status of HS link1 of a FEMB2 10: select the status of HS link2 of a FEMB2 11: select the status of HS link3 of a FEMB2 12: select the status of HS link0 of a FEMB3 13: select the status of HS link1 of a FEMB3 14: select the status of HS link2 of a FEMB3 15: select the status of HS link3 of a FEMB3
0x12 (18)	TS_latch	R/W	8	0: Hold time stamp counter 1: update time stamp counter real time
0x12 (18)	ERR_CNT_RST	R/W	15	1: reset timestamp counter, CHKSUM error counter, Frame error counter, header error counter. (Header error counter is meaningless for SBND FM, it is for ProtoDUNE FEMB)
0x13 (19)	LINK_DISABLE	R/W	15:0	Set to disable FEMB link going to NEVIS DAQ bit 0 = FEMB 0 link 0 1 = FEMB 0 link 1 2 = FEMB 0 link 2 3 = FEMB 0 link 3 4 = FEMB 1 link 0 4 = FEMB 1 link 1 ……. 14 = FEMB 3 link 2 15 = FEMB 3 link 3

ADDRESS	NAME	R/W	BIT	Description
0x14 (20)	TX_PACK_Stream_EN	R/W	0	0 (default) : enable data stream transmission to Nevis DAQ 1: disable data stream transmission to Nevis DAQ
0x14 (20)	NEVIS_SYNC	R/W	1	Force a resynchronization to NEVIS DAQ
0x14 (20)	tx_analogreset_EN	R/W	2	Transmitter analog reset enable
0x14 (20)	tx_digitalreset_EN	R/W	3	Transmitter digital reset enable
0x14 (20)	pll_powerdown_EN	R/W	4	Transmitter PLL power down
0x14 (20)	QSFP_RST	R/W	8	0 (default), 1: reset
0x15 (21)	-NOT USED-			Reserved
0x16 (22)	-NOT USED-			Reserved
0x17 (23)	EEPROM_ADDR	R/W	15:0	EEPROM ADDRESS (32bit words)
0x17 (23)	EEPROM_RD	R/W	16	Set then clear to generate a read operation result stored in register 0x19
0x17 (23)	EEPROM_WR	R/W	17	Set then clear to generate a write operation
0x17 (23)	LOAD_EE_DATA	R/W	31	Set then clear to reload the values stored in the EEPROM to the FPGA
0x18 (24)	EEPROM_WR_DATA	R/W	31:0	Data to write to EEPROM.
0x19 (25)	EEPROM_RD_DATA	R	31:0	Value returned from EEPROM after a EEPROM_RD
0x1A (26)	FPGA_F_OP_CODE	R/W	7:0	Set this to the proper FLASH OP-CODE (ALTERA EPCS) OP_CODES 0x02 = Write memory -- write enable must be set 0x03 = Read memory 0x04 = Disable Write Enable 0x05 = Read Status 0x06 = Write Enable (use before write @ bulk erase) 0xAB = Read Silicon ID 0xC7 = Erase bulk (write enable must be set)
0x1A (26)	F_FLASH_OP	R/W	8	Set this bit to start FPGA FLASH operation (user must clear) (ALTERA EPCS)

ADDRESS	NAME	R/W	BIT	Description
0x1B (27)	FPGA_F_ADDR	R/W	23:0	Set for start address of the FPGA FLASH 256 byte operation (ALTERA EPCS)
0x1C (28)	JTAG_EEPROM	W	0	Enable Flash programming mode or allow eeprom to be seen on JTAG scan.
0x1C (28)	FPGA_F_STATUS	R	1:0	Status returned by FPGA FLASH after operation Bit 0 = Write in progress Bit 1 = Write enable latch bit set (ALTERA EPCS)
0x1D (29)	-NOT USED-			Reserved
0x1E (30)	UDP_EN_WR_RDBK	R/W	0	Set to enable Write echo mode
0x1E (30)	UDP_REGISTER RESPONCE_PORT	R/W	1	Response port = 0x7d10 + (lowest octet of the IP address).
0x1F (31)	UDP_FRAME_SIZE	R/W	11:0	Default value: 0x1FB Other value: 0xEFB
0x20 (32)	HEADER_ERROR	R	15:0	Header error counter (not used in SBND FEMB)
0x20 (32)	ADC_ERROR	R	31:16	P1 ADC synchronization (not used in SBND FEMB)
0x21 (33)	LINK_SYNC_STATUS	R	31:0	High-speed link status, 2bits per link, 8 bits per FEMB 0 = Link down 1 = Link up
0x22 (34)	CHKSUM_ERROR	R	15:0	FEMB link checksum error counter Select link by using register 0x12
0x22 (34)	TIME_STAMP	R	31:16	FEMB link Time stamp counter Select link by using register 0x12
0x23 (35)	FRAME_ERROR	R	15:0	FEMB link Frame error counter Select link by using register 0x12
0x23 (35)	TS_ERROR	R	31:16	FEMB link Time stamp error counter Select link by using register 0x12
0x24 (36)	EQ_LOS_BRD0_RX	R	3:0	Equalizer status of FEMB0, 1 bit per link 0 = Link down 1 = Link up
0x24 (36)	EQ_LOS_BRD1_RX	R	7:4	Equalizer status of FEMB1, 1 bit per link 0 = Link down 1 = Link up

ADDRESS	NAME	R/W	BIT	Description
0x24 (36)	EQ_LOS_BRD2_RX	R	11:8	Equalizer status of FEMB2, 1 bit per link 0 = Link down 1 = Link up
0x24 (36)	EQ_LOS_BRD3_RX	R	15:12	Equalizer status of FEMB3, 1 bit per link 0 = Link down 1 = Link up
0x25 (37)	/	/	/	reserved
0x26 (38)	Start_MON_ADC	W	0	Start a conversion cycle of monitoring ADC. Suggest send 4 commands as below: Addr=0x38 write 0x01 Addr=0x38 write 0x00 Addr=0x38 write 0x01 Addr=0x38 write 0x00
0x26 (38)	Mon_ADC output	R	31:16	Monitor ADC for WIB SLOT0 (FEMB0)
0x26 (38)	Mon_ADC output	R	15:0	Monitor ADC for WIB SLOT1(FEMB1)
0x27 (39)	Mon_ADC output	R	31:16	Monitor ADC for WIB SLOT2 (FEMB2)
0x27 (39)	Mon_ADC output	R	15:0	Monitor ADC for WIB SLOT3(FEMB3)
0x28 (40)	-NOT USED-			Reserved
0x29 (41)	STATUS COUNTER SELECT	R/W	7:0	Link status counters 0 = SI5344_LOL_CNT 1-8 = FEM_SOP_CNT(X) 9-16 = FEM_BAD_PKT_CNT(X) 17 = FEMB_WR_strb_CNT 18 = FEMB_RDBK_strb_CNT Others = 0xDEADBEEF
0x2A (42)	STATUS COUNTER DATA	R	31:0	Counter Data Value selected by register 0x29 “STATUS COUNTER SELECT"
0xFF(255)	FIRMWARE VERSION	R	15:0	Firmware version number
0xFF(255)	WIB SLOT NUMBER	R	23:16	WIB WEIC slot location
0xFF(255)	WIB CRATE NUMBER	R	31:24	Number set on PTC DIP SWITCH
0x100(256)	FIRMWARE TRACKER	R	31:0	value increments on every compilation
0x101(257)	COMPILATION DATE	R	31:0	Value viewed in HEX
0x102(258)	COMPILATION TIME	R	31:0	Value viewed in HEX

ADDRESS	NAME	R/W	BIT	Description
0x200 - 0x2FF (512-767)	WIB_FAKE_DATA ODD	R/W	23:0	Fake data generator Odd channels
0x300 - 0x3FF	WIB_FAKE_DATA EVEN	R/W	23:0	Fake data generator even channels
0x400 - 0x4ff	FPGA-FIRMWARE-UPDATE MEMORY WRITE	R/W	31..0	Storage for Writing FPGA EPCS 256 bytes
0x400 - 0x4ff	FPGA-FIRMWARE-UPDATE MEMORY READ	R/W	31..0	Storage for read back of FPGA EPCS 256 bytes

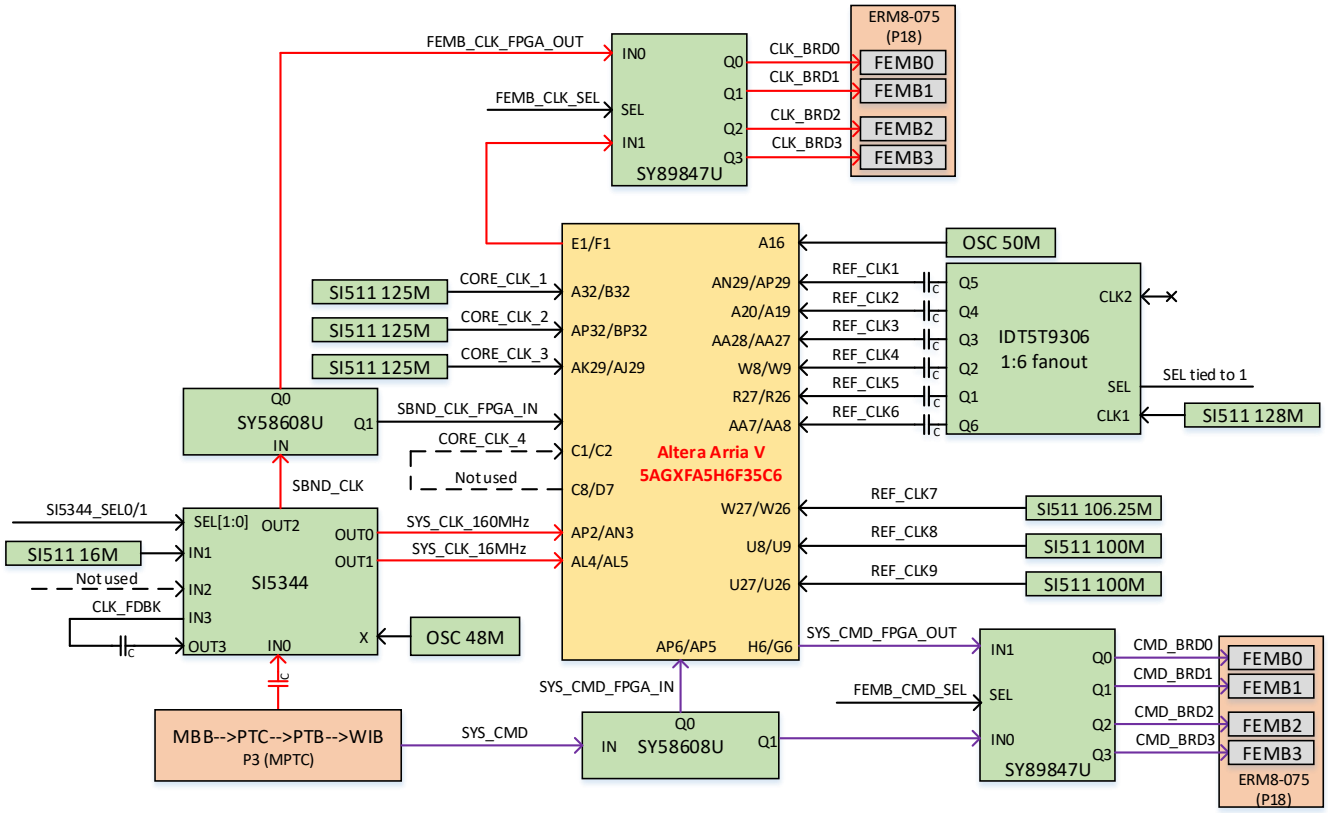


Figure 3 SBND WIB Clock and Command Distribution Diagram

SBND MBB

Register Map version 107

ADDRESS	NAME	R/W	BIT	Description
0 (0x00)	SYS_RESET	W	0	Set to reset entire system (AUTO Clears)
0 (0x00)	REG_RESET	W	1	Set to reset system registers (AUTO Clears)
0 (0x00)	UDP_RESET	W	2	Set to reset UDP interface (AUTO Clears)
0 (0x00)	ALG_RESET	W	0	Set to reset MBB state machine (AUTO Clears)
1 (0x01)	CALIBRATION_PULSE	R/W	0	Transition form 0 to 1 will generate a calibration signal sent to all FEMB's
1 (0x01)	TIMESTAMP_RESET	R/W	1	Transition form 0 to 1 will generate a timestamp reset signal to all FEMB's
1 (0x01)	STOP_FEMB_DAQ	R/W	2	Transition form 0 to 1 will stop all FEMB's generating data (Synchronous stop)
1 (0x01)	START_FEMB_DAQ	R/W	3	Transition form 0 to 1 will start all FEMB's generating data (Synchronous start)
2 (0x02)	DISABLE EXTERNAL CALIBRATION	R/W	0	This will mask the front panel MBB calibration pulse input (Set to disable LEMO input)
3 (0x03)	PLL_CLOCK_SELECT	R/W	0	0 = External clock input -- 16MHz from Nevis 1 = Internal 16MHz clock -- (external clock must be present to switch to internal clock)
3 (0x03)	PLL_RESET	R/w	1	Set to reset PLL -- does not auto clear
4 (0x04)	PTC_DATA_ADDRESS	R/W	3..0	(SET to 0x02) to control WIB POWER
4 (0x04)	PTC_CRATE_ADDRESS	R/W	7..4	PTC Crate address: set by PTC dipswitch Allows system to control each PTC individually
5 (0x05)	PTC_DATA	R/W	15..0	Data word to be sent to PTC (To control PTC POWER on PTC register 0x02 Set BIT to disable WIB BIT 0 = WIB 1 POWER DISABLE BIT 1 = WIB 2 POWER DISABLE BIT 2 = WIB 3 POWER DISABLE BIT 3 = WIB 4 POWER DISABLE BIT 4 = WIB 5 POWER DISABLE BIT 5 = WIB 6 POWER DISABLE
6 (0x06)	PTC_WR_REG	R/W	0	Transition form 0 to 1 will send data to the PTC
7 (0x07)	PULSE_SRC_SELECT	R/W	3..0	Select source for Calibration pulse 0x0 = LEMO INPUT

				0x1 = MBB internal pulse generator 0x2-0xF = DO NOT USE ..
8 (0x08)	PULSE_PERIOD	R/W	31..0	Set the period of the MBB internal test pulse 0 = 0 1 = 10ns 2= 20ns ..
9 (0x09)	PLL_ACTIVE_CLK	R	0	This is used to verify which clock is being used by the PLL 0 = External clock 1 = Internal 16Mhz clock
9 (0x09)	PLL_CLK_STATUS	R	5..4	0 = clock good 1= clock bad Bit 4 = External clock Bit 5 = Internal clock
10 (0x0A)	UDP_EN_WR_RDBK	R/W	0	Set to enable Write echo mode
10 (0x0A)	UDP_REGISTER_RESPONCE_PORT	R/W	1	For firmware version 106 BU – style response echoed on port 0x7d01 for write and 0x7d02 for reads For Firmware version 107 Response port = 0x7d10 + (lowest octet of the IP address).
0xFF (255)	FIRMWARE VERSION	R	15:0	Firmware version number
0x100 (256)	FIRMWARE TRACKER	R	31:0	value increments on every compilation
0x101 (257)	COMPILATION DATE	R	31:0	Value viewed in HEX
0x102 (258)	COMPILATION TIME	R	31:0	Value viewed in HEX