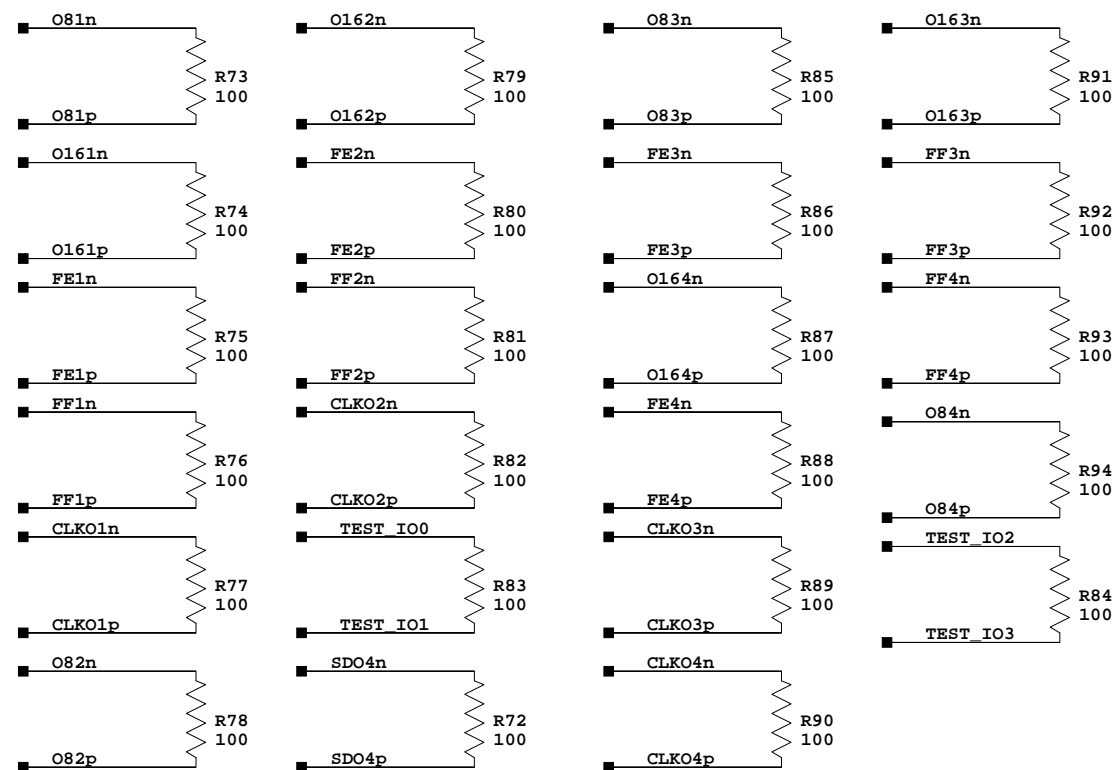
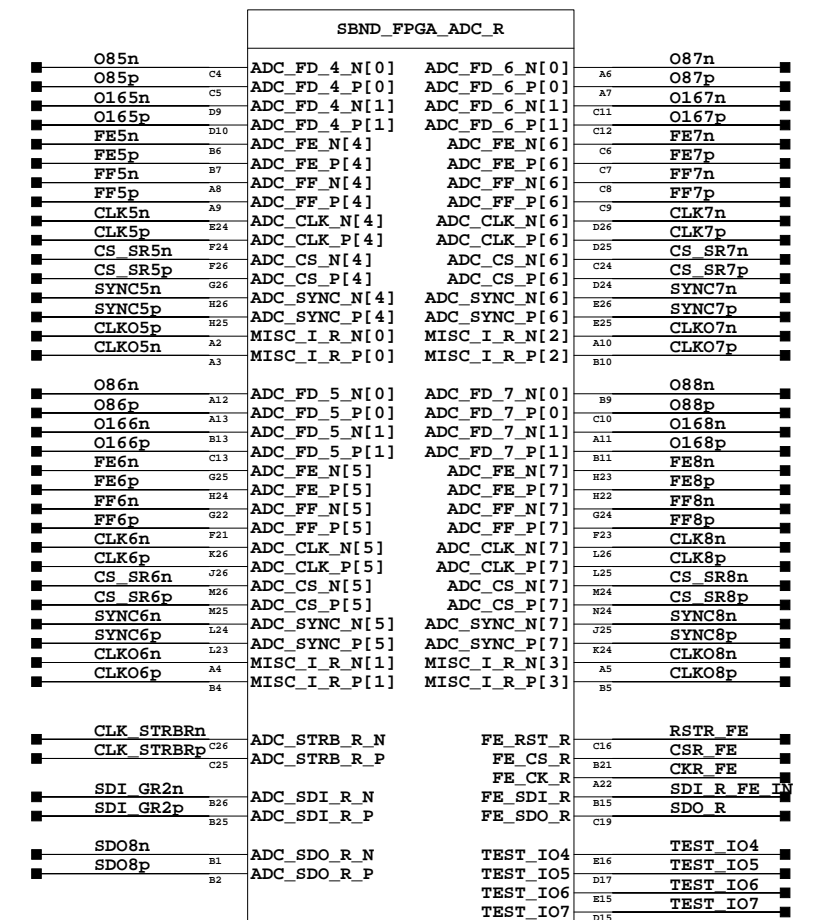
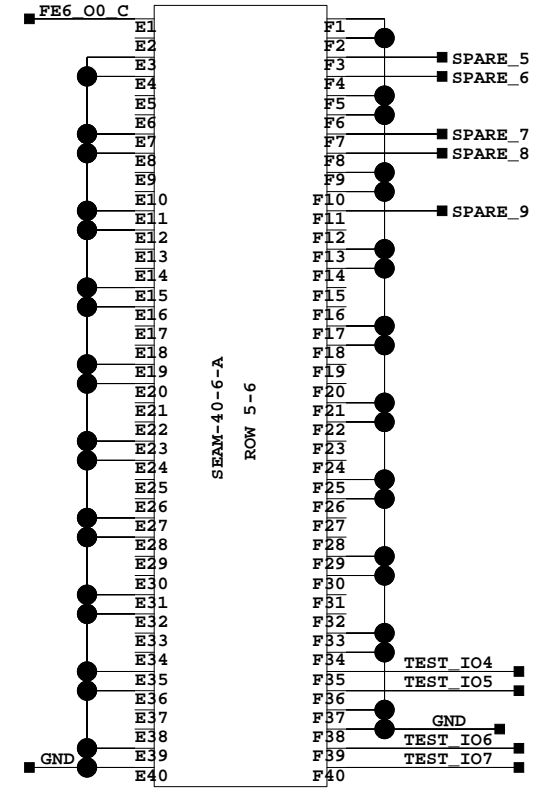
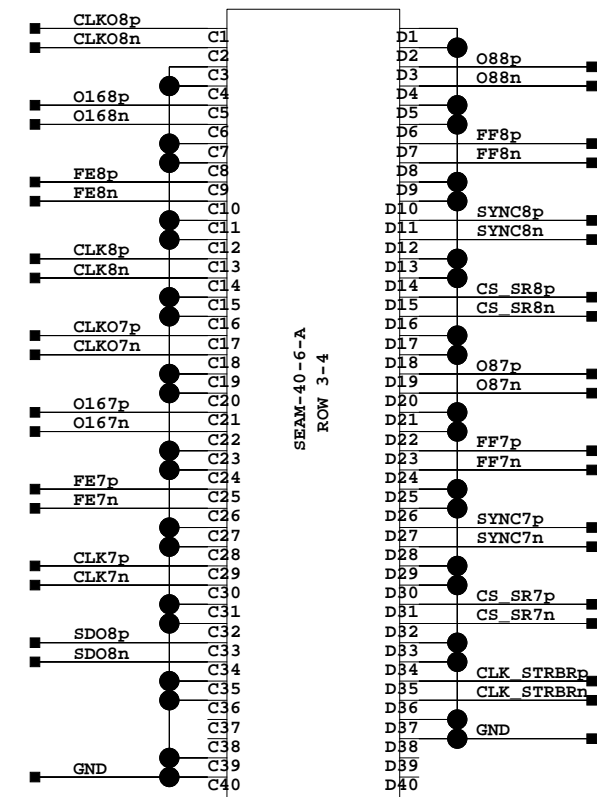
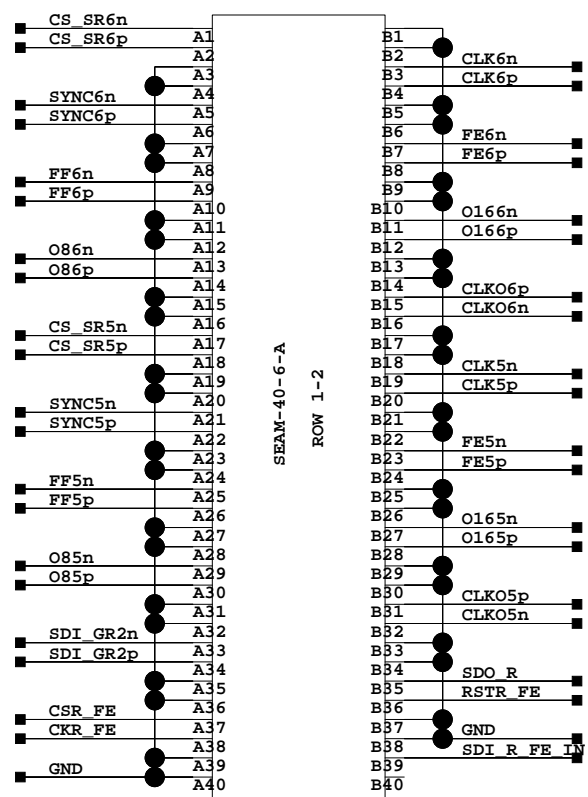
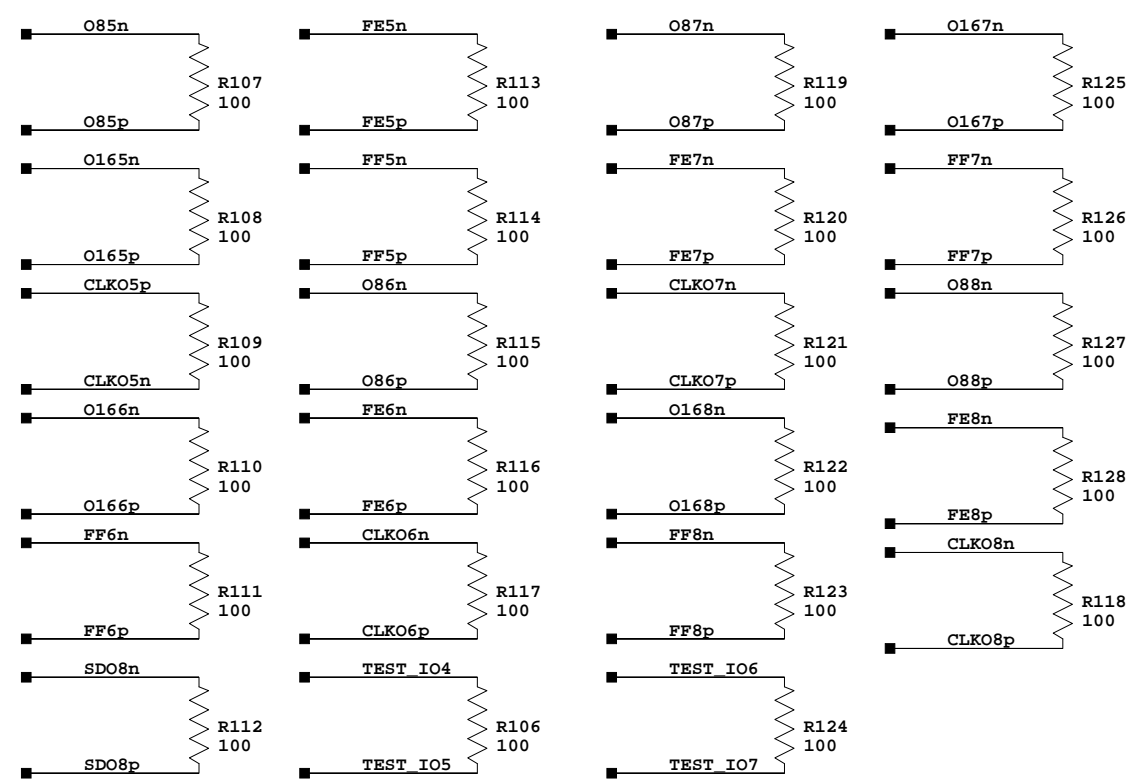


**LVDS TERMINATION
PLACE UNDER FPGA**





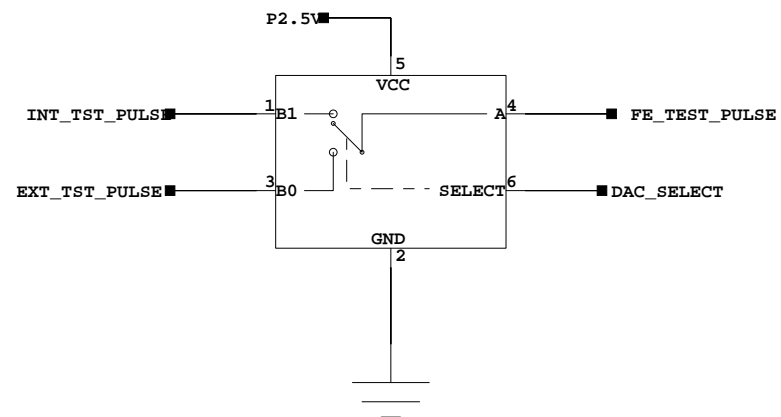
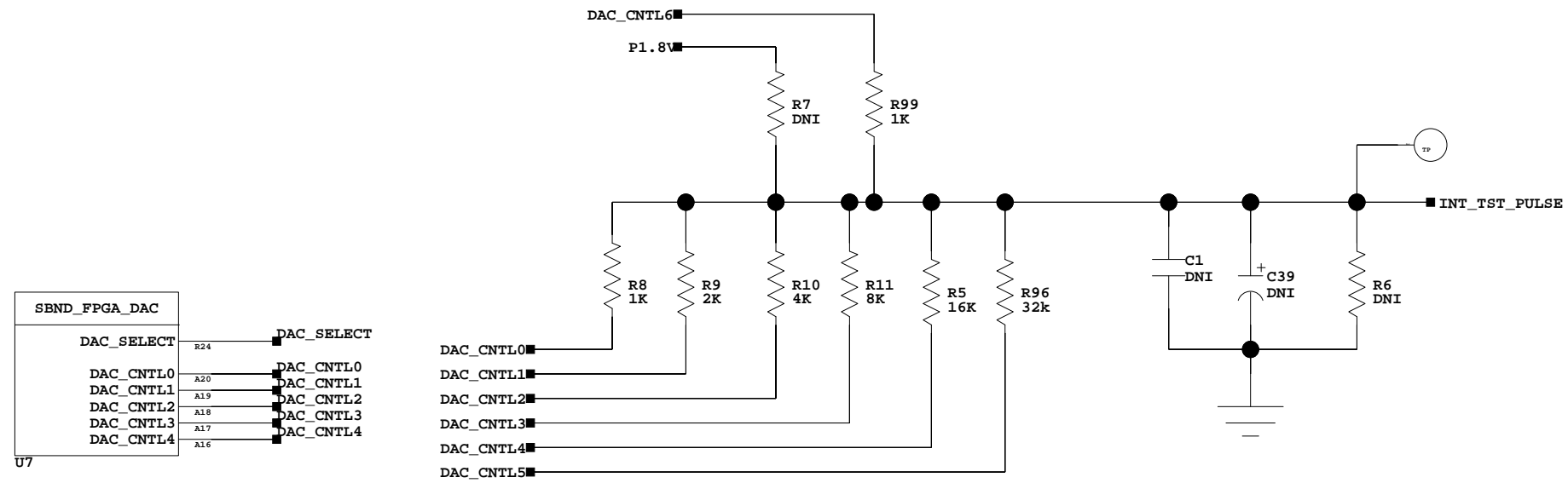
LVDS TERMINATION PLACE UNDER FPGA



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DUNE_ADC_IO_R

Date: 29/07/2016:16:43 DRAWN BY: Jack Fried

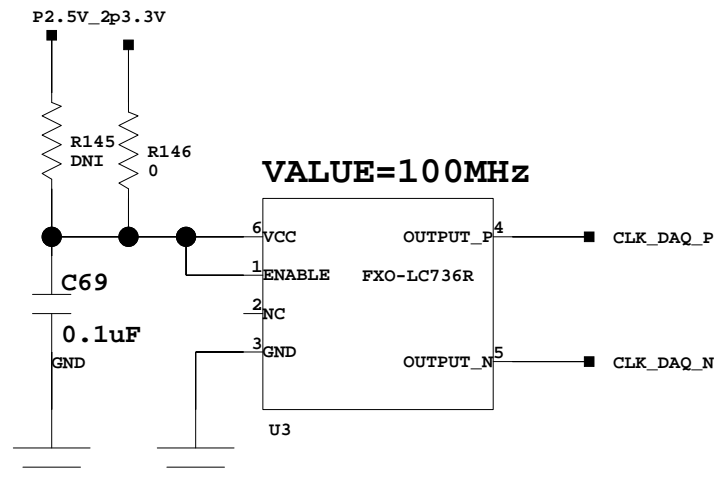
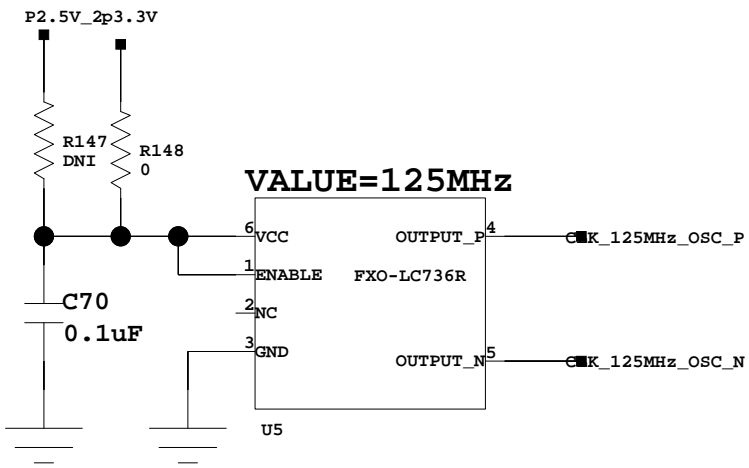
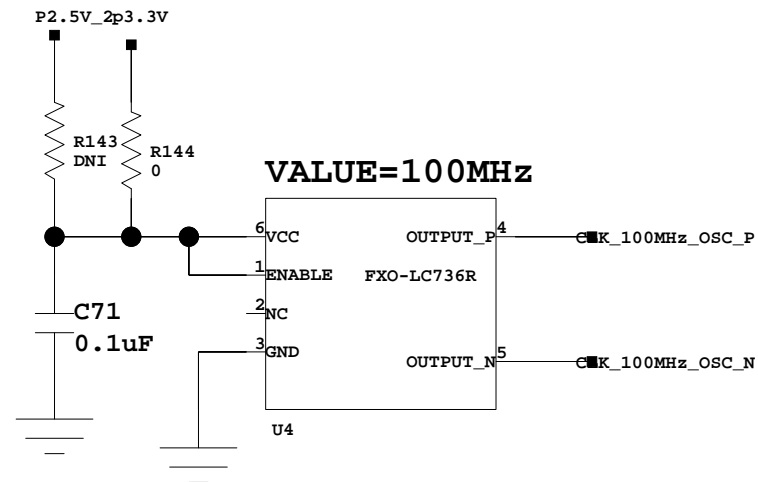


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DUNE_DAC

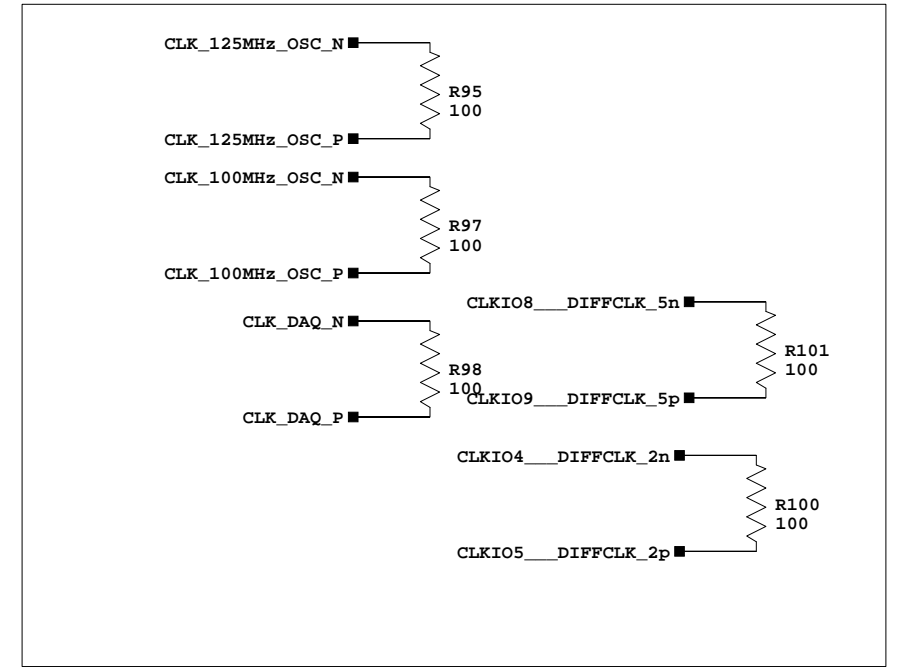
Date: 21/09/2016:14:03

DRAWN BY: Jack Fried

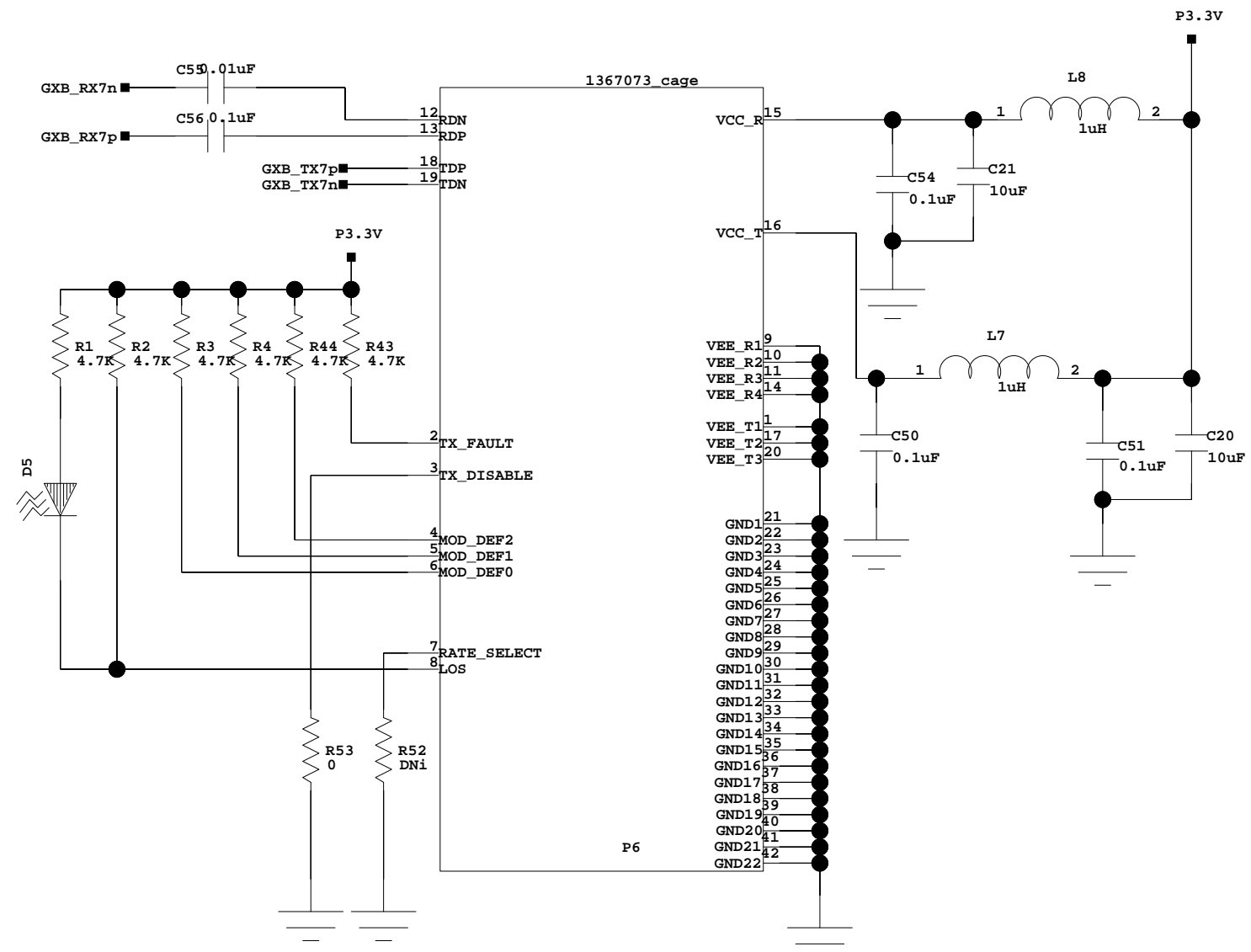
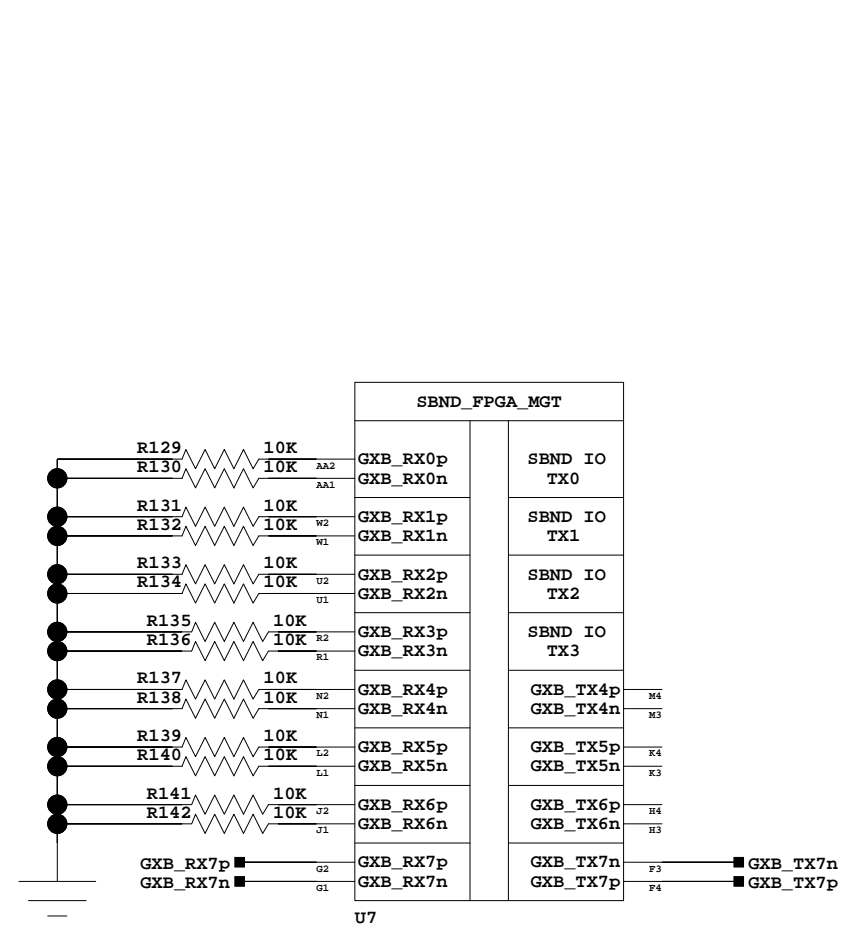


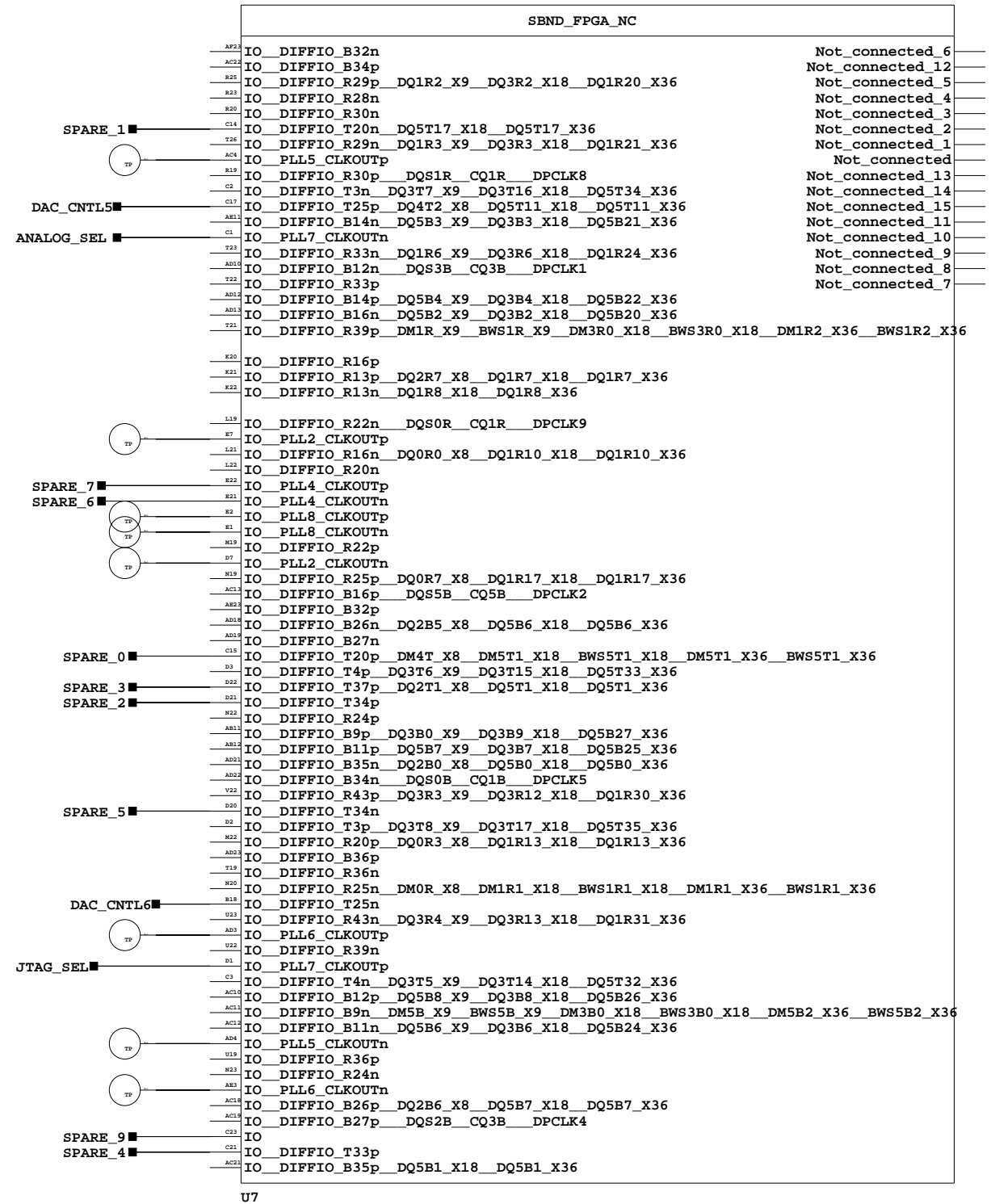
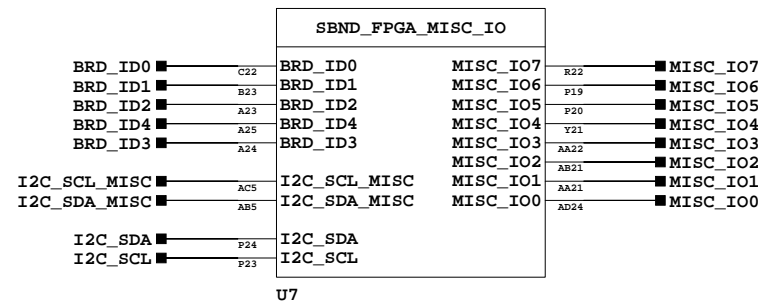
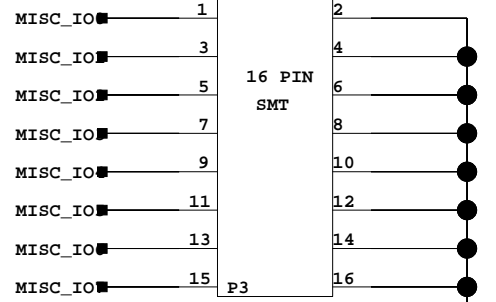
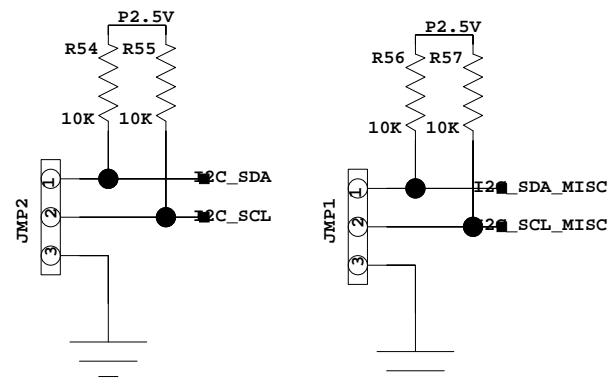
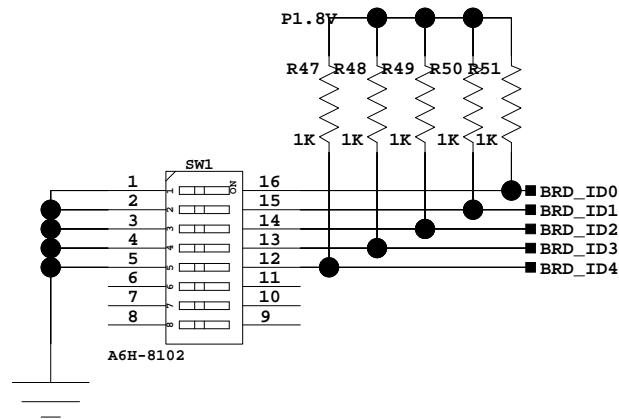
SBND_FPGA_CLK		
SBND_CLK_T	U9	CLK_125MHz_OSC_N
SBND_CLK_T	T9	CLK_125MHz_OSC_P
CLK_125MHz_OSC_N	K9	CLK_125M_spare_N
CLK_125MHz_OSC_P	L9	CLK_125M_spare_P
CLK_100MHz_OSC_N	T15	CLK_100MHz_OSC_N
CLK_100MHz_OSC_P	T14	CLK_100MHz_OSC_P
CLK_DAQ_N	N26	CLK_DAQ_N
CLK_DAQ_P	N25	CLK_DAQ_P
CLK_DAQ_N	L14	CLK_EXT_N
CLK_DAQ_P	L15	CLK_EXT_P
CLK_100MHz_OSC_N	K10	REFCLK4n
CLK_100MHz_OSC_P	L10	REFCLK4p
I2C_SCL_DIF	U10	REFCLK1n
I2C_SCL_DIF	T10	REFCLK1p
CLKIO4_DIFFCLK_2n	P26	CLKIO4_DIFFCLK_2n
CLKIO5_DIFFCLK_2p	R26	CLKIO5_DIFFCLK_2p
CLKIO8_DIFFCLK_5n	A14	CLKIO8_DIFFCLK_5n
CLKIO9_DIFFCLK_5p	B14	CLKIO9_DIFFCLK_5p

U7



UNDER FPGA



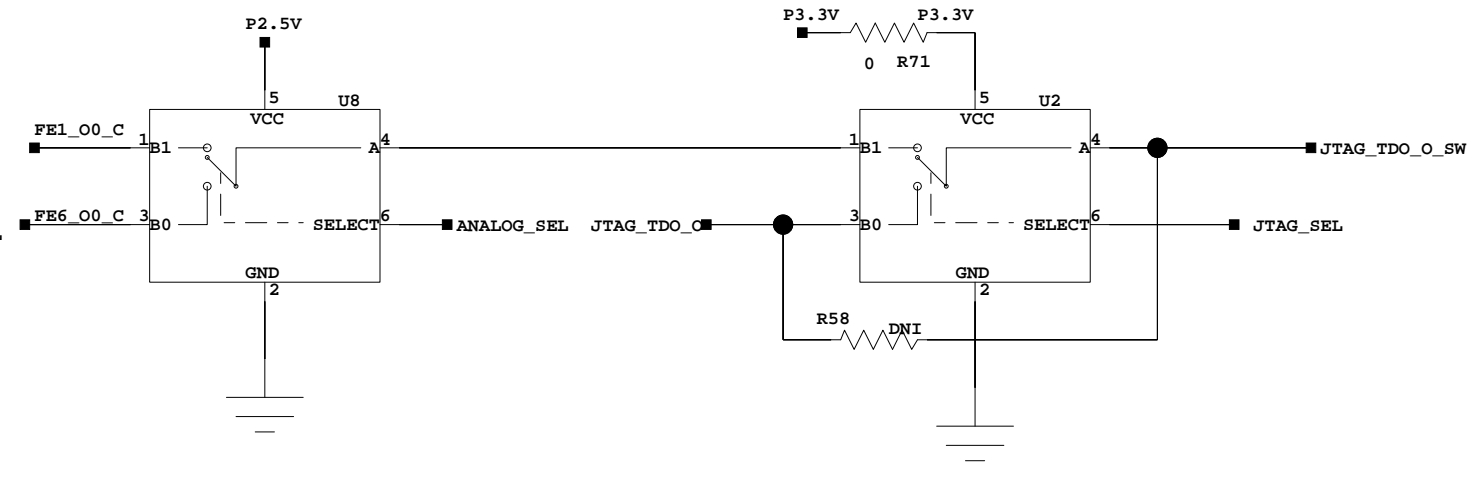
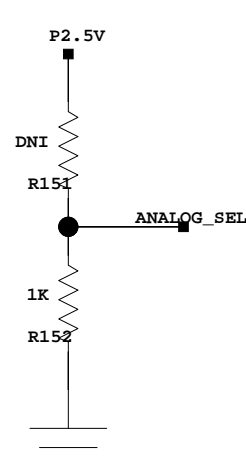
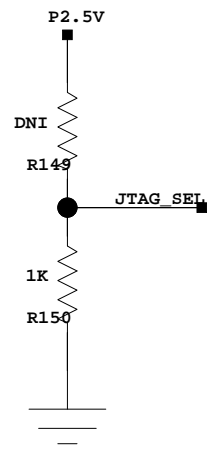
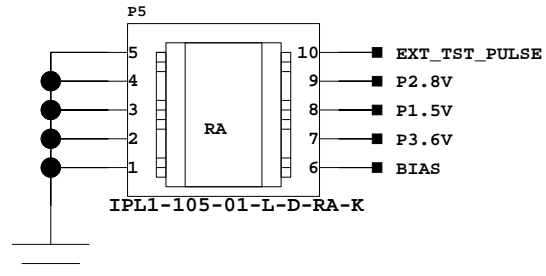


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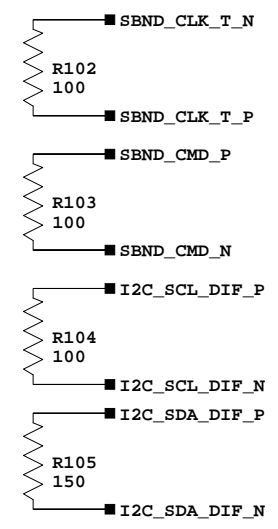
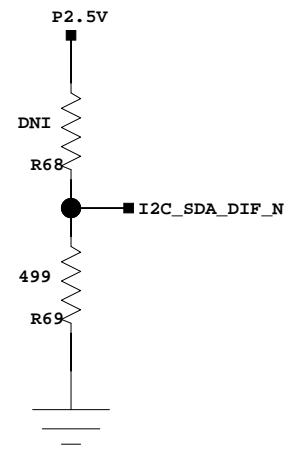
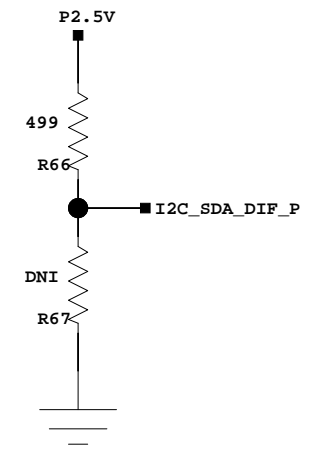
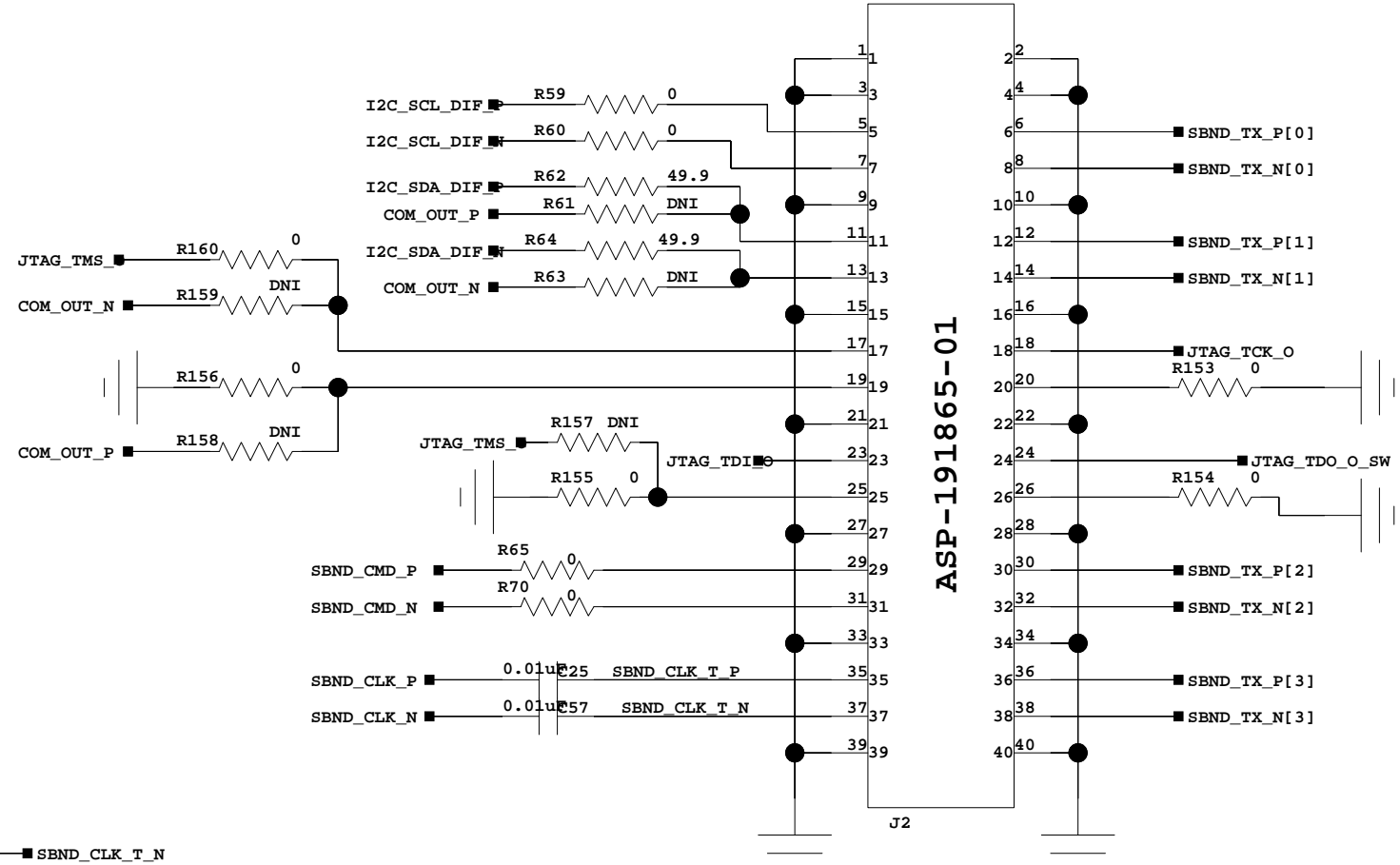
DUNE_MISC_IO

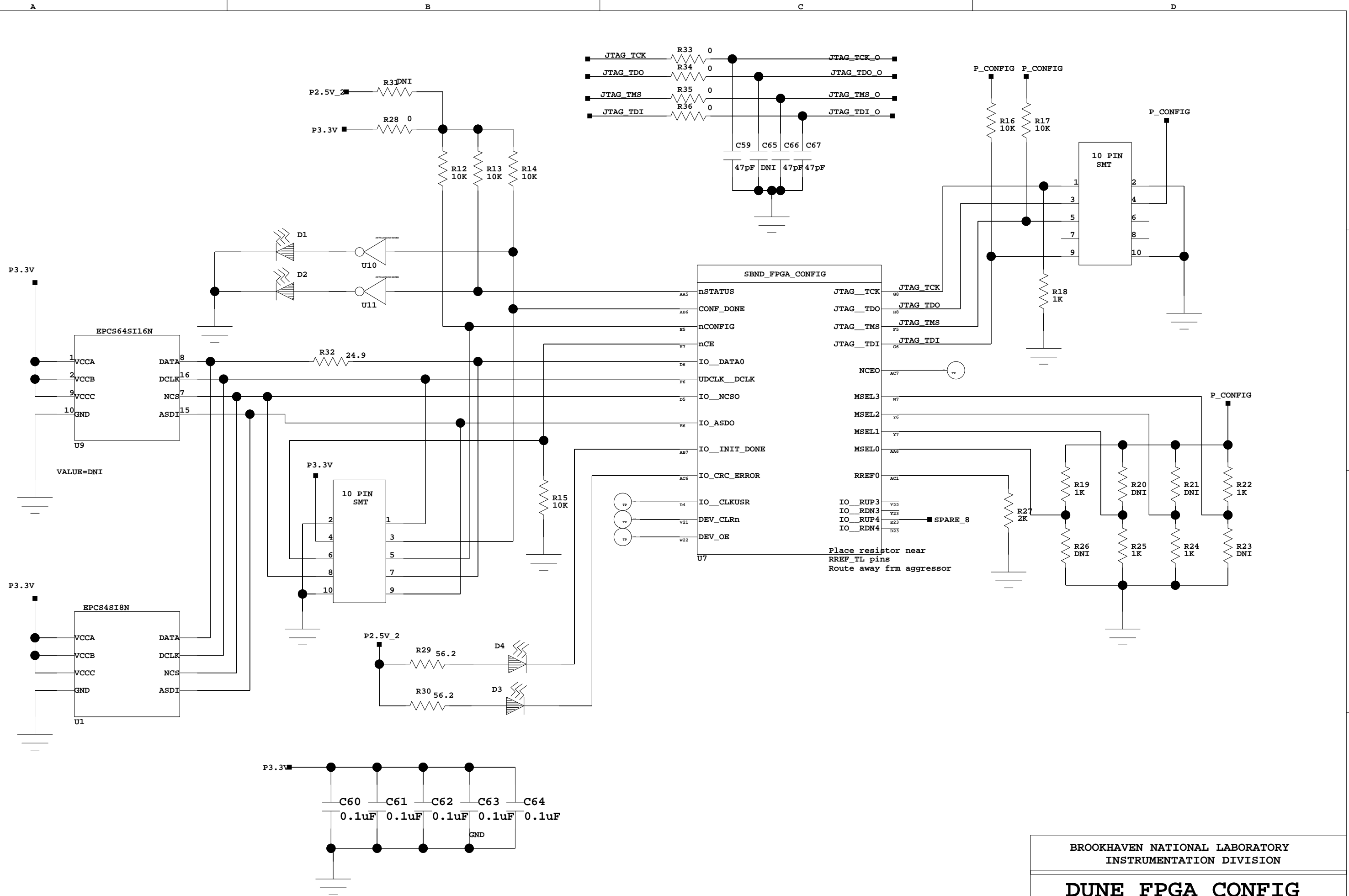
Date: 07/09/2016:11:37

DRAWN BY: Jack Fried



SBND_FPGA_IO		
SBND_TX_N[0]	Y3	SBND_TX_N[3]
SBND_TX_P[0]	Y4	SBND_TX_P[3]
SBND_TX_N[1]	V3	SBND_TX_N[2]
SBND_TX_P[1]	V4	SBND_TX_P[2]
SBND_TX_N[2]	T3	SBND_TX_N[1]
SBND_TX_P[2]	T4	SBND_TX_P[1]
SBND_TX_N[3]	F3	SBND_TX_N[0]
SBND_TX_P[3]	F4	SBND_TX_P[0]
SBND_CLK_N	AF14	SBND_CLK_N
SBND_CLK_P	AF13	SBND_CLK_P
SBND_CMD_N	AD14	SBND_CMD_N
SBND_CMD_P	AC14	SBND_CMD_P
I2C_SCL_DIF_P	AF2	I2C_SCL_DIF_P
I2C_SCL_DIF_N	AF3	I2C_SCL_DIF_N
I2C_SDA_DIF_P	AE1	I2C_SDA_DIF_P
I2C_SDA_DIF_N	AE2	I2C_SDA_DIF_N
COM_OUT_N	J23	COM_OUT_N
COM_OUT_P	K23	COM_OUT_P



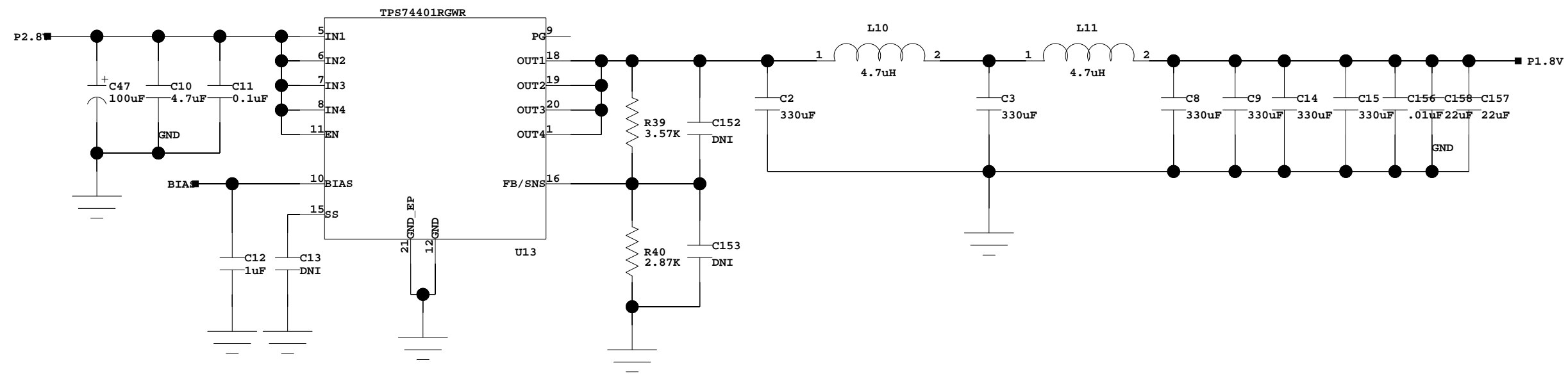
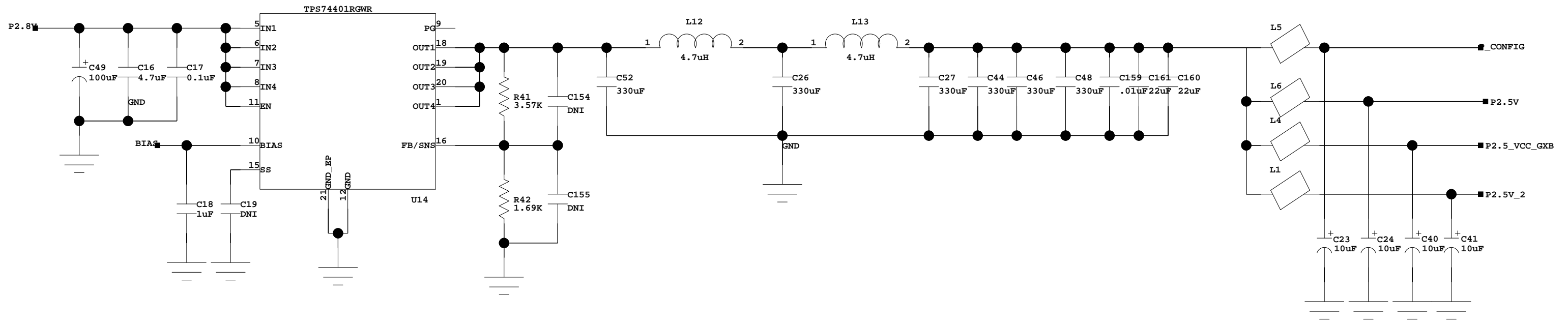


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DUNE_FPGA_CONFIG

Date: 29/07/2016:16:30

DRAWN BY: Jack Fried

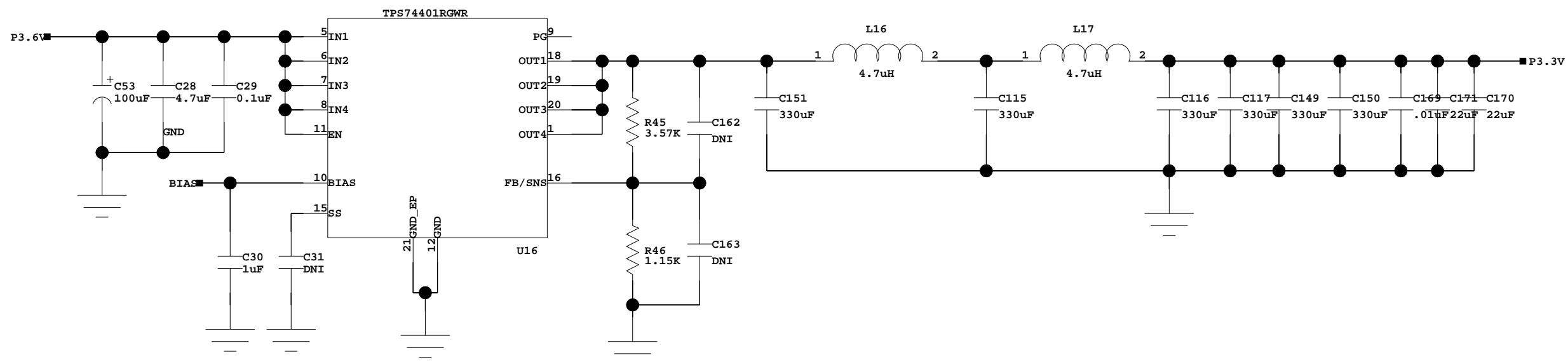
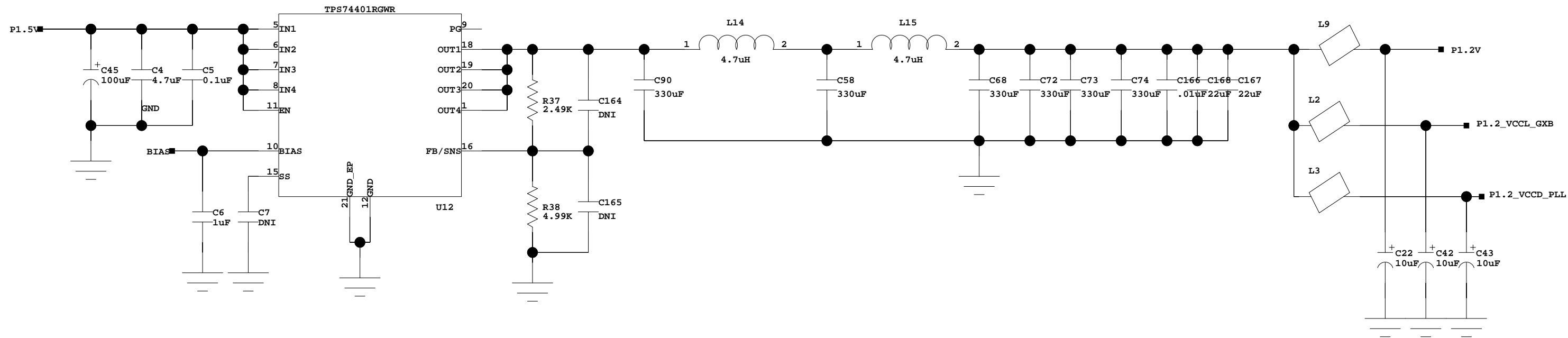


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DUNE_PWR_1

Date: 08/06/2016:12:43

DRAWN BY: Jack Fried

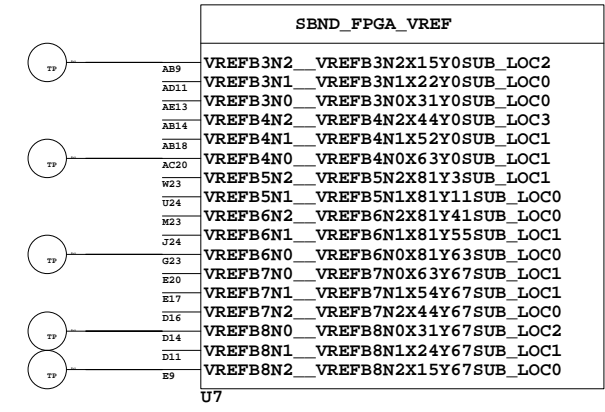
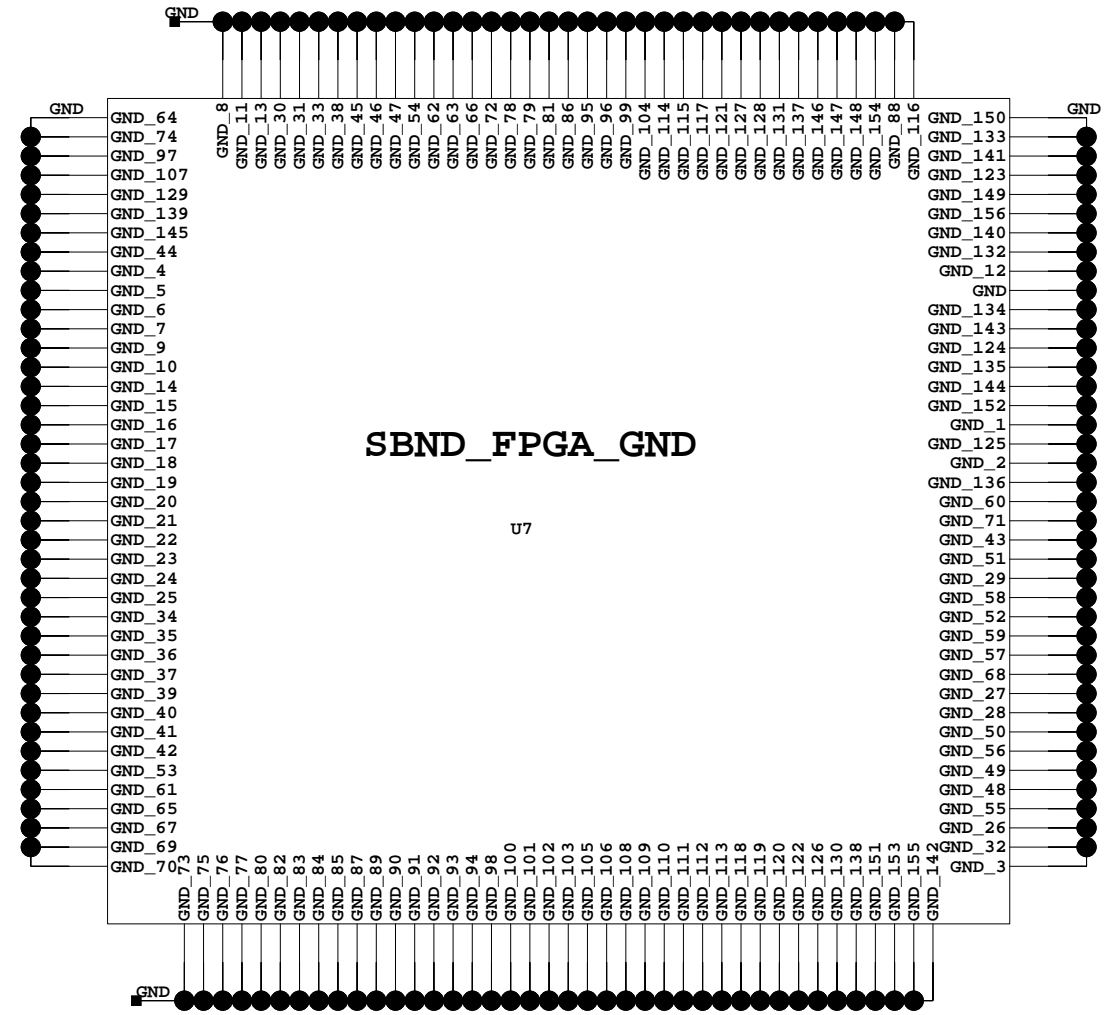
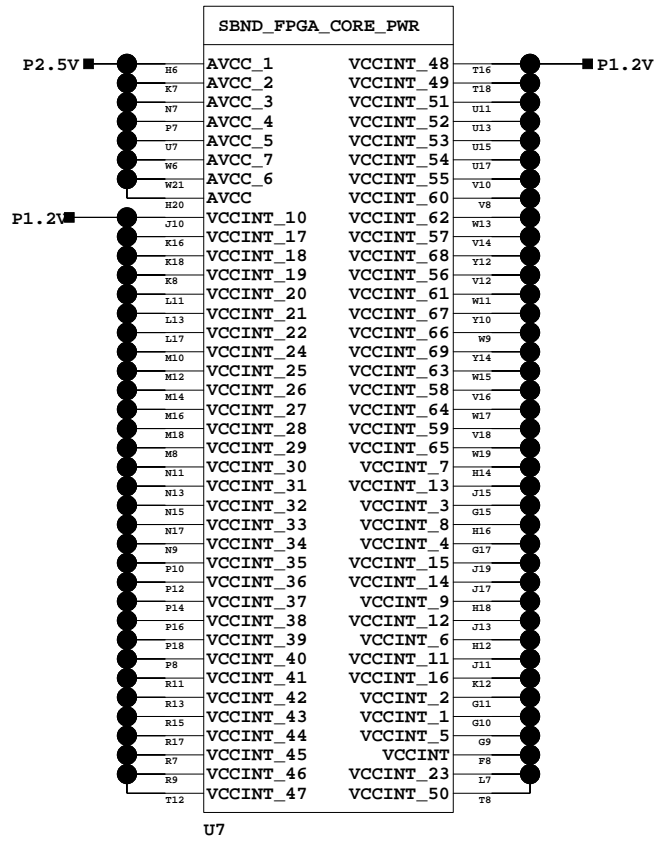
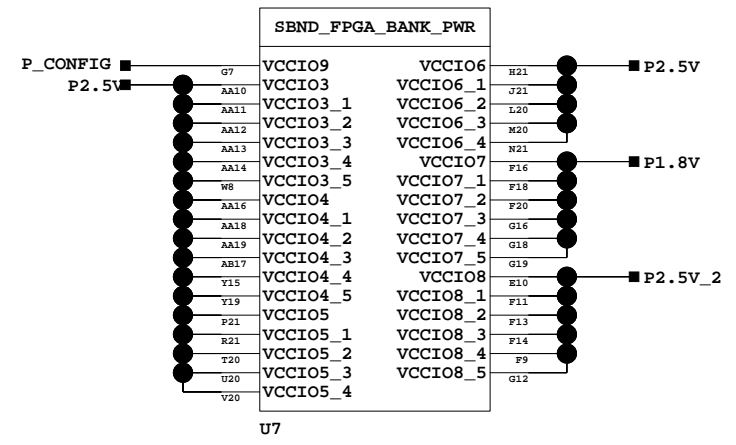
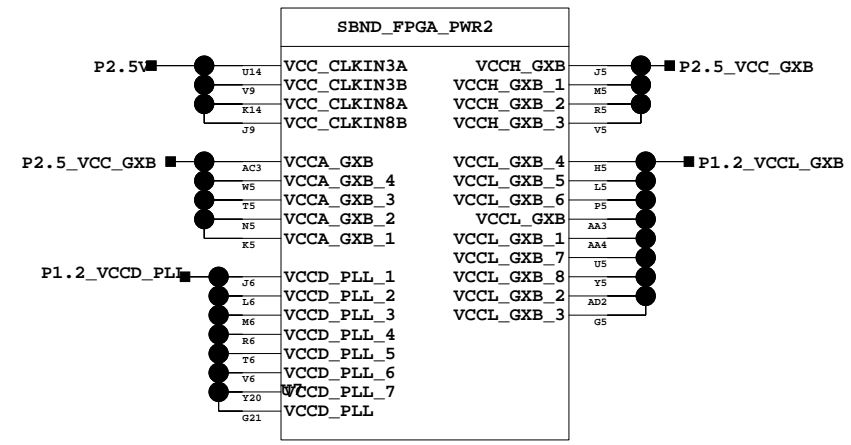


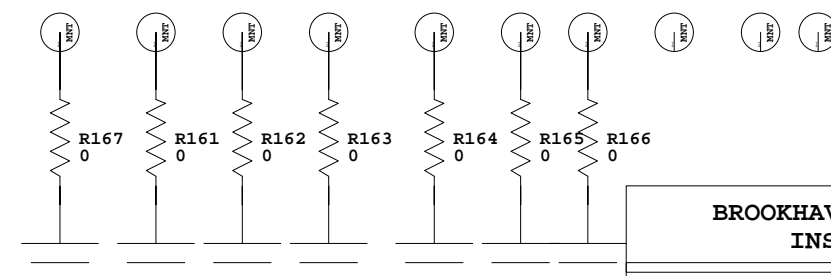
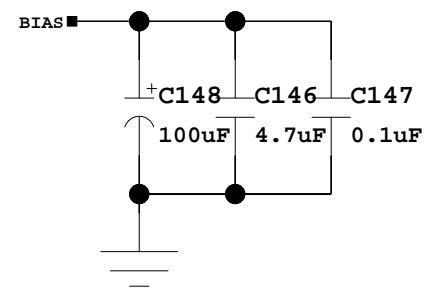
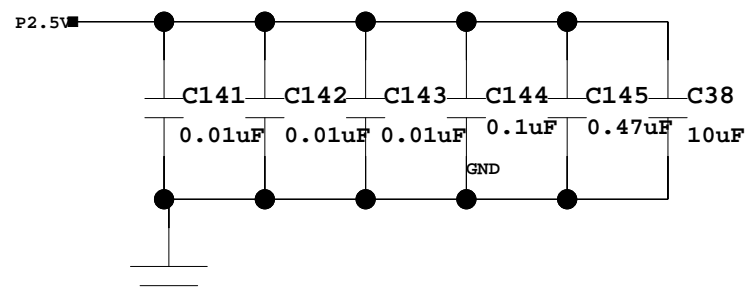
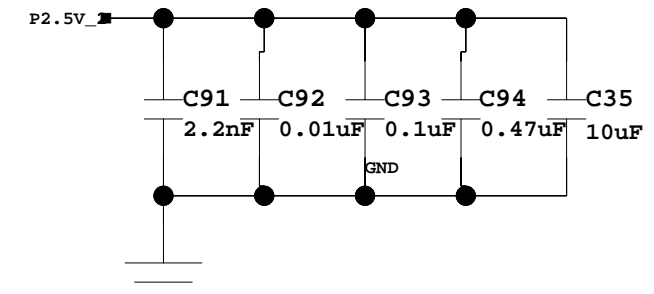
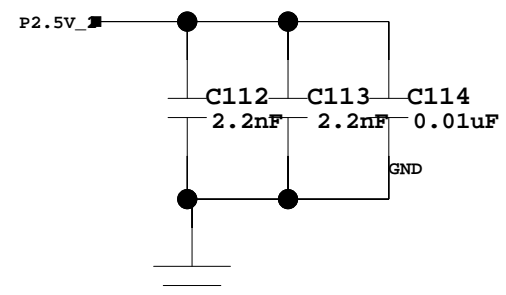
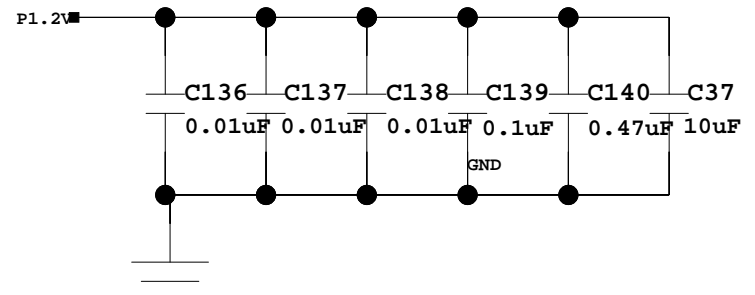
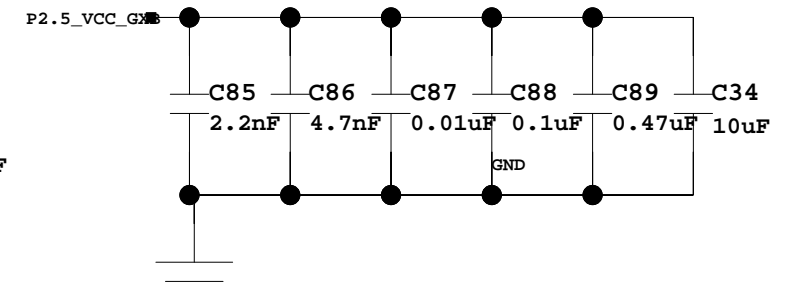
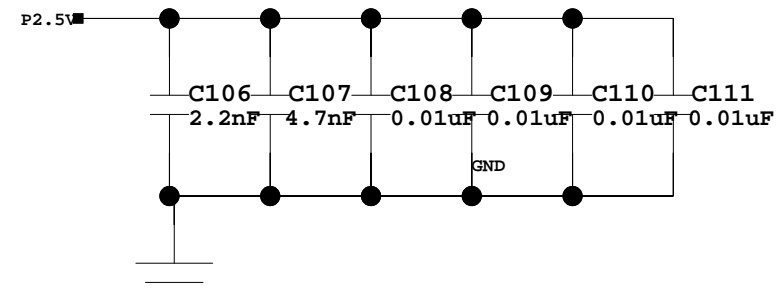
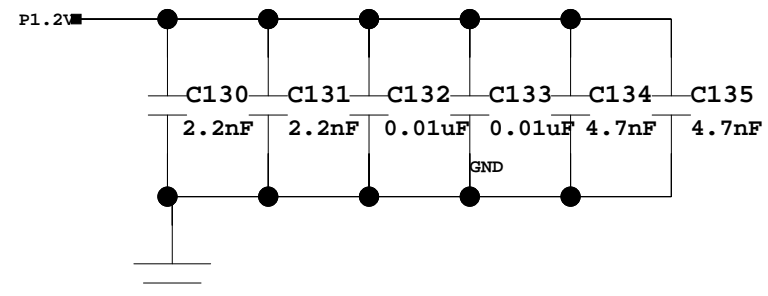
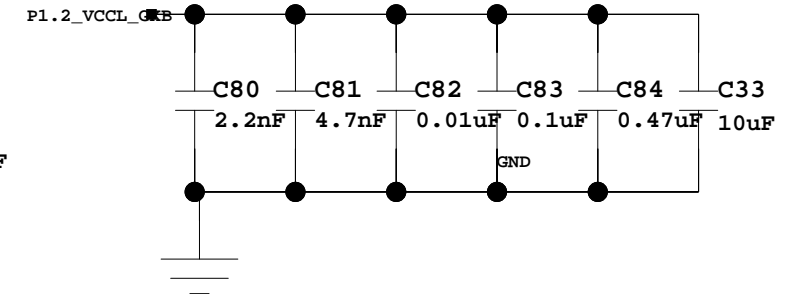
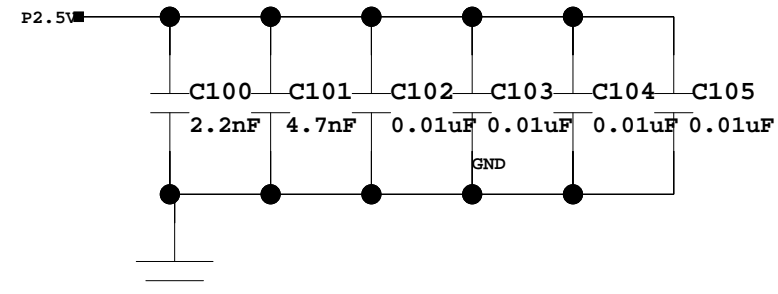
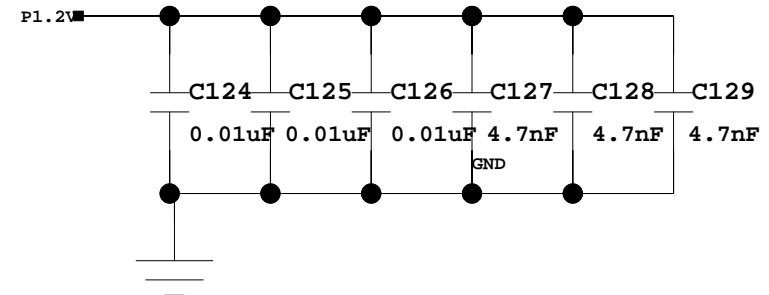
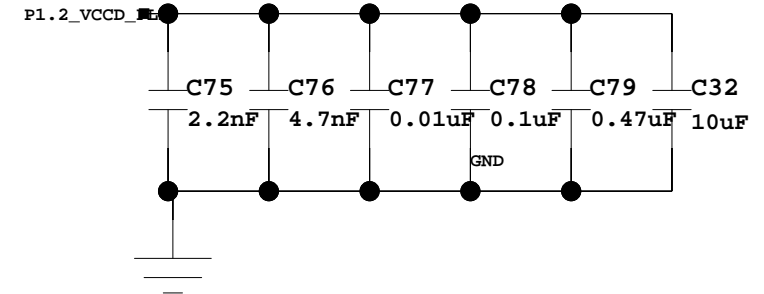
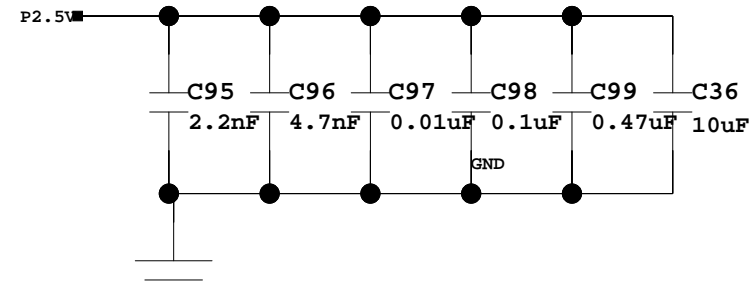
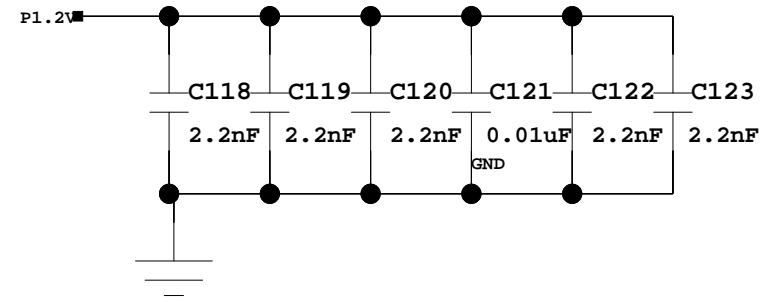
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DUNE_PWR_2

Date: 08/06/2016:12:43

DRAWN BY: Jack Fried





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DUNE_FPGA_DECOUPLING

Date: 17/06/2016:13:58

DRAWN BY: Jack Fried