SBND/ProtoDUNE_FPGA

Register Map version 202 (DRAFT)

ADDRESS	NAME	R/W	BIT	Description
0 (0x00)	SYS_RESET	W	0	Set to reset entire system (AUTO Clears)
0 (0x00)	REG_RESET	W	1	Set to reset system registers (AUTO Clears)
0 (0x00)	TIME_STAMP RESET	W	2	Set to " SBND time stamp reset
1 (0x01)	ADC_ASIC RESET	W	0	Set to reset ADC ASIC'S (AUTO Clears)
1 (0x01)	FE_ASIC_RESET	W	1	Set to reset FE ASIC's (AUTO Clears)
2 (0x02)	WRITE_ADC_ASIC SPI	W	0	Set to write ADC ASIC SPI (AUTO Clears)
2 (0x02)	WRITE_FE_ASIC SPI	W	1	Set to write FE ASIC SPI (AUTO Clears)
3 (0x03)	ADC_ASIC_DISABLE	R/W	7..0	Set to disable ADC ASIC readout and insert 0x00 (default) "TEST PATTERN" Set bit 0 for ASIC 1 Set bit 1 for ASIC 2 Set bit 2 for ASIC 3 ..... Set bit 7 for ASIC 8
3 (0x03)	DATA_TEST PATTERN	R/W	27..16	12 bit test pattern to insert into data stream. 0x123 (default)
3 (0x03)	ADC_TEST_PATTER N_ENABLE	R/W	31	Set to force ADC to send test pattern (used in old ADC ASIC) 0x0 (default)
4 (0x04)	ADC_LATCH_LOC_0	R/W	7..0	Set value to correct for ADC bit shift (ADC 1)
4 (0x04)	ADC_LATCH_LOC_1	R/W	15..8	Set value to correct for ADC bit shift (ADC 2)
4 (0x04)	ADC_LATCH_LOC_2	R/W	23..16	Set value to correct for ADC bit shift (ADC 3)
4 (0x04)	ADC_LATCH_LOC_3	R/W	31..24	Set value to correct for ADC bit shift (ADC 4)
5 (0x05)	TEST_PULSE AMPLITUDE	R/W	5..0	SET to control 5 bit DAC for test pulse 0 = Disabled (default) 1 = DAC LSB (TBD) 2= .. ..

5 (0x05)	TEST_PULSE DELAY	R/W	15..8	Controls test pulse sample shift by 20ns steps 0 = 0 1 = 20ns 2= 40ns .. ..
5 (0x05)	TEST_PULSE PERIOD	R/W	31..16	Set to control test pulse period 0x0000 (default) (dependent on ADC SAMPLE RATE) 00 = 500nS , 666nS ,1uS , 2uS (LSB) 01 = 1uS , 1.33uS, 2uS, 4uS 02 = 1.5uS, 2nS, 3uS, 6uS ... ...
6 (0x06)	ADC_ASIC_CLK PHASE SELECT	R/W	7..0	Set to select clock phase Bit 0 = ASIC 1 0 = clock 0 deg 1 = clock 180 deg phase Bit 1 = ASIC 2 0 = clock 0 deg 1 = clock 180 deg phase Bit 2 = ASIC 3 0 = clock 0 deg 1 = clock 180 deg phase .. Bit 7= ASIC 8 0 = clock 0 deg 1 = clock 180 deg phase
6 (0x06)	ADC ASIC SYNC STATUS	R	31..16	Bit 16 = ASIC 1 link 1 sync status 0 = sync good Bit 17 = ASIC 1 link 2 sync status 0 = sync good Bit 18 = ASIC 2 link 1 sync status 0 = sync good Bit 19 = ASIC 2 link 2 sync status 0 = sync good .. .. .. Bit 28 = ASIC 7 link 1 sync status 0 = sync good Bit 29 = ASIC 7 link 2 sync status 0 = sync good Bit 30 = ASIC 8 link 1 sync status 0 = sync good Bit 31 = ASIC 8 link 2 sync status 0 = sync good
7 (0x07)	CHP_select	R/W	7..0	(GIG-E UDP) Select Chip data to be sent over UDP 0 = ASIC 1 1 = ASIC 2 2 = ASIC 3 .. .. 7 = ASIC 8
7 (0x07)	CHN_select	W	11..8	(GIG-E UDP) (will be overridden by register 17 bit 0) Select Channel data to be sent over UDP 0 = channel 1 1 = channel 2 2 = channel 3 .. .. 7 = channel 8
8	RESERVED	R/W	31..0	NOT USED (can be used for scratch pad)

(0x08)				
9 (0x09)	Stream_EN	R/W	0	Set to enable to enable high speed data If set to zero high speed link will only send k codes
9 (0x09)	PRBS_EN	R/W	1	Set to send PRBS test pattern
9 (0x09)	CNT_EN	R/W	2	Set to send test counter
9 (0x09)	ADC_DATA_EN	R/W	3	Set to send ADC DATA (must be set for normal operation)
10 (0x0A)	FPGA_F_OP_CODE	R/W	7..0	Set this to the proper FLASH OP-CODE (ALTERA EPCS) OP_CODES 0x00 (default) 0x02 = Write memory -- write enable must be set 0x03 = Read memory 0x04 = Disable Write Enable 0x05 = Read Status 0x06 = Write Enable (use before write @ bulk erase) 0xAB = Read Silicon ID (result is stored in status reg) 0xC7 = Erase bulk (write enable must be set)
10 (0x0A)	FPGA_F_STRT_OP	R/W	8	Set this bit to start FPGA FLASH operation (user must clear) (ALTERA EPCS) 0x0 (default)
11 (0x0B)	FPGA_F_ADDR	R/W	23..0	Set for start address of the FPGA FLASH 256 byte operation (ALTERA EPCS) 0x0 (default)
12 (0x0C)	FPGA_F_status	R	1..0	Status returned by FPGA FLASH after operation Bit 0 = Write in progress Bit 1 = Write enable latch bit set (ALTERA EPCS) 0x0 (default)
13 (0x0D)	FPGA_F_ENABLE	W	0	Set to enable EPCS FPGA flash programmer
14 (0x0E)	ADC_LATCH_LOC_4	R/W	7..0	Set value to correct for ADC bit shift (ADC 5)
14 (0x0E)	ADC_LATCH_LOC_5	R/W	15..8	Set value to correct for ADC bit shift (ADC 6)
14 (0x0E)	ADC_LATCH_LOC_6	R/W	23..16	Set value to correct for ADC bit shift (ADC 7)
14 (0x0E)	ADC_LATCH_LOC_7	R/W	31..24	Set value to correct for ADC bit shift (ADC 8)
15 (0x0F)	RESERVED	---	31..0	DO NOT USE
16 (0x10)	FPGA_TP_EN	R/W	0	Set to enable FPGA calibration DAC
16 (0x10)	ASIC_TP_EN	R/W	1	Set to enable ASIC calibration (calibration pulse will be sent to ASIC ck pin)
17 (0x11)	DAC_SELECT	R/W	0	(GIG-E UDP) SET to override register 7 channel select and send all ASIC data for selected chip

18 (0x12)	INT_TP_EN	R/W	0	Set to enable internal pulse generator Period set by register 5
18 (0x12)	EXT_TP_EN	R/W	1	Set to allow test pulses to be received by external timing control interface (register 5 delay & amplitude can be used)
19 (0x13)	FEMB_TST_MODE	R/W	0	Set to enable data test mode (ADC ASIC data is replaced with data stored in FEMB memory location (0x300 - 0x3ff)
20 (0x14)	TX_PLL_RESET	R/W	0	Set to reset FPGA transceiver PLL
20 (0x14)	TX_DIGITAL_RST	R/W	1	Set to reset FPGA transceiver digital logic
256 (0x100)	SCRATCH_PAD	R/W	31..0	Register scratch pad 0x0 (default)
257 (0x101)	VERSION ID	R	15 ..0	FIRMWARE VERSION ID
257 (0x101)	BOARD ID	R	31 ..16	Board ID read form dip switch
512-547 (0x200- 0x223)	ADC ASIC SPI WRITE DATA	R/W	31..0	ADC ASIC SPI data to written into the ASICs (1096) bits (137 bits per ASIC) 0x0 (default)
552-587 (0x228- 0x24B)	ADC ASIC SPI READBACK	R/W	31..0	ADC ASIC SPI data to written into the ASICs (1096) bits (137 bits per ASIC) 0x0 (default)
592-627 (0x250- 0x273)	FE ASIC SPI WRITE DATA	R/W	31..0	ADC ASIC SPI data to written into the ASICs (1088) bits (136 bits per ASIC) 0x0 (default)
632-667 (0x278 - 0x29B)	FE ASIC SPI READBACK	R/W	31..0	ADC ASIC SPI data to written into the ASICs (1088) bits (136 bits per ASIC) 0x0 (default)
512-520 (0x200 - 0x208)	FPGA_F_WR MEMORY	R/W	31..0	Storage for Writing FPGA EPCS 256 bytes 0x0 (default)
576-584 (0x240 - 0x248)	FPGA_F_RD MEMORY	R/W	31..0	Storage for read back of FPGA EPCS 256 bytes 0x0 (default)
768-1023 (0x300 - 0x3FF)	WFM_GEN_DATA	R/W	23..0	256 samples of TEST pattern memory for fake data generator (must set registers 3 bits 7..0 and must set register 19 Bits (11..0) = odd channels Bits(23..12) = even channels