ProtoDUNE FPGA Mezzanine

Register Map version 323

ADDRESS	NAME	R/W	BIT	Description
0 (0x00)	SYS_RESET	W	0	Set to reset entire system (AUTO Clears)
0 (0x00)	REG_RESET	W	1	Set to reset system registers (AUTO Clears)
0 (0x00)	TIME_STAMP RESET	W	2	Set to " ProtoDUNE time stamp reset
1 (0x01)	ADC_ASIC RESET	W	0	Set to reset ADC ASIC'S (AUTO Clears)
1 (0x01)	FE_ASIC_RESET	W	1	Set to reset FE ASIC's (AUTO Clears)
2 (0x02)	WRITE_ADC_ASIC SPI	W	0	Set to write ADC ASIC SPI (AUTO Clears)
2 (0x02)	WRITE_FE_ASIC SPI	W	1	Set to write FE ASIC SPI (AUTO Clears)
3 (0x03)	ADC_ASIC_DISABLE	R/W	7..0	Set to disable ADC ASIC readout and insert 0x00 (default) "TEST PATTERN" Set bit 0 for ASIC 1 Set bit 1 for ASIC 2 Set bit 2 for ASIC 3 ..... Set bit 7 for ASIC 8
3 (0x03)	DATA_TEST PATTERN	R/W	27..16	12 bit test pattern to insert into data stream. 0x123 (default)
3 (0x03)	ADC_TEST_PATTERN_ENABLE	R/W	31	Set to force ADC to send test pattern (used in old ADC ASIC) 0x0 (default)
4 (0x04)	ADC_LATCH_LOC_0	R/W	7..0	Set value to correct for ADC bit shift (ADC 1)
4 (0x04)	ADC_LATCH_LOC_1	R/W	15..8	Set value to correct for ADC bit shift (ADC 2)
4 (0x04)	ADC_LATCH_LOC_2	R/W	23..16	Set value to correct for ADC bit shift (ADC 3)
4 (0x04)	ADC_LATCH_LOC_3	R/W	31..24	Set value to correct for ADC bit shift (ADC 4)
5 (0x05)	TEST_PULSE AMPLITUDE	R/W	5..0	SET to control 5 bit DAC for test pulse 0 = Disabled (default) 1 = DAC LSB (TBD) 2= .. ..

5 (0x05)	TEST_PULSE DELAY	R/W	15..8	Controls test pulse sample shift by 10ns steps 0 = 0 1 = 10ns 2= 20ns .. ..
5 (0x05)	TEST_PULSE PERIOD	R/W	31..16	Set to control test pulse period 0x0000 (default) (dependent on ADC SAMPLE RATE) 00 = 500nS 01 = 1uS 02 = 1.5uS ... ...
6 (0x06)	ADC_ASIC_CLK PHASE SELECT	R/W	7..0	Set to select clock phase works with register 0x0F (ADC_ASIC_CLK PHASE, ADC_ASIC_CLK PHASE2) Bit 0 ASIC 1 (0,0) = clock 0 deg (0,1) = clock 90 deg (1,0) = clock 180 deg (1,1) = clock 270 deg Bit 1 ASIC 2 (0,0) = clock 0 deg (0,1) = clock 90 deg (1,0) = clock 180 deg (1,1) = clock 270 deg Bit 2 ASIC 3 (0,0) = clock 0 deg (0,1) = clock 90 deg (1,0) = clock 180 deg (1,1) = clock 270 deg Bit 3 ASIC 4 (0,0) = clock 0 deg (0,1) = clock 90 deg (1,0) = clock 180 deg (1,1) = clock 270 deg . . Bit 7 ASIC 7 (0,0) = clock 0 deg (0,1) = clock 90 deg (1,0) = clock 180 deg (1,1) = clock 270 deg
6 (0x06)	ADC ASIC SYNC STATUS	R	31..16	Bit 16 = ASIC 1 link 1 sync status 0 = sync good Bit 17 = ASIC 1 link 2 sync status 0 = sync good Bit 18 = ASIC 2 link 1 sync status 0 = sync good Bit 19 = ASIC 2 link 2 sync status 0 = sync good .. .. .. Bit 28 = ASIC 7 link 1 sync status 0 = sync good Bit 29 = ASIC 7 link 2 sync status 0 = sync good Bit 30 = ASIC 8 link 1 sync status 0 = sync good Bit 31 = ASIC 8 link 2 sync status 0 = sync good
7 (0x07)	CHP_select	R/W	7..0	(NOT USED IN V323)
7 (0x07)	CHN_select	W	11..8	(NOT USED IN V323)
8 (0x08)	WIB_MODE	R/W	0	(NOT USED IN V323)
8 (0x08)	ADC_ENABLE_REG	R/W	4	When set to 1 the ADC Readout is enabled (default = 1) When set to 0 the Readout is disabled

				(this register can override the timing system disable command)
8 (0x08)	FEMB SYSTEM CLOCK SWITCH	R/W	16	Set to use onboard oscillator instead of system clock (Should ONLY be used for testing FEMB)
9 (0x09)	Stream_EN	R/W	0	Set to enable to enable high speed data If set to zero high speed link will only send k codes
9 (0x09)	PRBS_EN	R/W	1	Set to send PRBS test pattern
9 (0x09)	CNT_EN	R/W	2	Set to send test counter
9 (0x09)	ADC_DATA_EN	R/W	3	Set to send ADC DATA (must be set for normal operation)
10 (0x0A)	FPGA_F_OP_CODE	R/W	7..0	Set this to the proper FLASH OP-CODE (ALTERA EPCS) OP_CODES 0x00 (default) 0x02 = Write memory -- write enable must be set 0x03 = Read memory 0x04 = Disable Write Enable 0x05 = Read Status 0x06 = Write Enable (use before write @ bulk erase) 0xAB = Read Silicon ID (result is stored in status reg) 0xC7 = Erase bulk (write enable must be set)
10 (0x0A)	FPGA_F_STRT_OP	R/W	8	Set this bit to start FPGA FLASH operation (user must clear) (ALTERA EPCS) 0x0 (default)
11 (0x0B)	FPGA_F_ADDR	R/W	23..0	Set for start address of the FPGA FLASH 256 byte operation (ALTERA EPCS) 0x0 (default)
12 (0x0C)	FPGA_F_status	R	1..0	Status returned by FPGA FLASH after operation Bit 0 = Write in progress Bit 1 = Write enable latch bit set (ALTERA EPCS) 0x0 (default)
13 (0x0D)	FPGA_F_ENABLE	W	0	Set to enable EPCS FPGA flash programmer
14 (0x0E)	ADC_LATCH_LOC_4	R/W	7..0	Set value to correct for ADC bit shift (ADC 5)
14 (0x0E)	ADC_LATCH_LOC_5	R/W	15..8	Set value to correct for ADC bit shift (ADC 6)
14 (0x0E)	ADC_LATCH_LOC_6	R/W	23..16	Set value to correct for ADC bit shift (ADC 7)
14 (0x0E)	ADC_LATCH_LOC_7	R/W	31..24	Set value to correct for ADC bit shift (ADC 8)
15 (0x0F)	ADC_ASIC_CLK PHASE SELECT 2	R/W	7..0	Refer to register 6
16 (0x10)	FPGA_TP_EN	R/W	0	Set to enable FPGA calibration DAC
16 (0x10)	ASIC_TP_EN	R/W	1	Set to enable ASIC calibration (calibration pulse will be sent to ASIC ck pin)

16 (0x10)	DAC_SELECT	R/W	8	Selects analog pulse source going to FE ASIC 0 = FPGA Mezzanine on board DAC 1 = Analog pulse from the WIB
16 (0x10)	ANALOG SIGNAL_SEL	R/W	9	Not used
16 (0x10)	ANALOG/JTAG SELECT	R/W	10	Set to select analog monitor to be driven over JTAG TDO line
17 (0x11)	CHN_select_UDP	R/W	3..0	(NOT USED IN V323)
18 (0x12)	INT_TP_EN	R/W	0	Set to enable internal pulse generator Period set by register 5
18 (0x12)	EXT_TP_EN	R/W	1	Set to allow test pulses to be received by external timing control interface (register 5 delay & amplitude can be used)
19 (0x13)	FEMB_TST_MODE	R/W	0	Set to enable data test mode (ADC ASIC data is replaced with data stored in FEMB memory location (0x300 - 0x3ff)
20 (0x14)	TX_PLL_RESET	R/W	0	Set to reset FPGA transceiver PLL
20 (0x14)	TX_DIGITAL_RST	R/W	1	Set to reset FPGA transceiver digital logic
20 (0x14)	START FRAME MODE SELECT	R/W	4	Set to enable Cold data K-code format (BU FIRMWARE)
20 (0x14)	START FRAME SWAP	R/W	5	Set to reverse start bit location (BC3C) VS (3CBC) (for backward compatibility)
21 (0x15)	ADC_EXT_CLK PERIOD	R/W	15..0	V323 SETTINGS (Values change for compilations) SET TO = 0x0000
21 (0x15)	ADC_EXT_CLK CLOCK_INVERT	R/W	31..16	V323 SETTINGS (Values change for compilations) SET TO = 0x0063
22 (0x16)	ADC_EXT_CLK RESET_OFFSET	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x00
23 (0x17)	ADC_EXT_CLK RESET_WIDTH	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x90009
24 (0x18)	ADC_EXT_CLK READ_OFFSET	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x600060
25 (0x19)	ADC_EXT_CLK READ_WIDTH	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x40004
26 (0x1A)	ADC_EXT_CLK IDXM_OFFSET	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x2E002E
27 (0x1B)	ADC_EXT_CLK IDXM_WIDTH	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x360036
28 (0x1C)	ADC_EXT_CLK IDXL_OFFSET	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x600060
29 (0x1D)	ADC_EXT_CLK IDXL_WIDTH	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x40004
30 (0x1E)	ADC_EXT_CLK IDL_1_OFFSET	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0xA000A

31 (0x1F)	ADC_EXT_CLK IDL_1_WIDTH	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x250025
32 (0x20)	ADC_EXT_CLK IDL_2_OFFSET	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x600060
33 (0x21)	ADC_EXT_CLK IDL_2_WIDTH	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x40004
34 (0x22)	NOT USED	R/W	31..0	NOT USED
35 (0x23)	PLL_STEP0_L	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x9000B
36 (0x24)	PLL_STEP1_L	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0xC0007
37 (0x25)	PLL_STEP2_L	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x8000000A
38 (0x26)	PLL_STEP0_R	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x50001
39 (0x27)	PLL_STEP1_R	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x30004
40 (0x28)	PLL_STEP2_R	R/W	31..0	V323 SETTINGS (Values change for compilations) SET TO = 0x80040004
41 (0x29)	ADC_SYNC_MODE	R/W	1..0	ADC sampling clock synchronization select 00 = Normal -- Sync convert signal to 200MHz clk 01 = Free running -- No synchronization 10 = follow -- System convert signal passed to ADC with no synchronization to system clock 11 = Convert clock disabled
42 (0x2A)	FEMB_TST_SEL	R/W	3..0	Test mode (Fake data Generator) 0 = Normal Mode (Real Data) 1 = Test Pattern loaded to all channels (from REG 0x03) 2 = Waveform data generator data loaded in memory location (0x300 -0x3FF) 3 = Channel indicator 0xA,B,C Where A = FEM NUMBER (REG 42(7..0)) B = Chip number C = Channel number 4 = Channel indicator 0xA,B,C Where A = 4 bit counter B = Chip number C = Channel number
42 (0x2A)	FEMB_NUMBER	R/W	7..4	Used with FEMB_TST_SEL mode 3
43 (0x2B)	TEST_PULSE_WIDTH	R/W	15..0	Test pulse width control. (Default 0xA00) 0 = 10ns 1 = 20ns 2 = 30ns
256 (0x100)	SCRATCH_PAD	R/W	31..0	Register scratch pad 0x0 (default)

257 (0x101)	VERSION ID	R	15 ..0	FIRMWARE VERSION ID
257 (0x101)	BOARD ID	R	31 ..16	Board ID read form dip switch
258 (0x102)	COMPILED VERSION	R	31..0	Complied version number (auto increments)
259 (0x103)	DATE COMPILED	R	31..0	Date Complied (in HEX)
260 (0x104)	TIME COMPILED	R	31..0	Time Complied (in HEX)
512-547 (0x200-0x248)	ASIC SPI WRITE DATA	R/W	31..0	ASIC SPI data to be written into the ASICs
552-587 (0x250-0x298)	ASIC SPI READBACK	R/W	31..0	ASIC SPI data to be read back
512-520 (0x200 - 0x208)	FPGA_F_WR MEMORY	R/W	31..0	Storage for Writing FPGA EPCS 256 bytes 0x0 (default)
576-584 (0x240 - 0x248)	FPGA_F_RD MEMORY	R/W	31..0	Storage for read back of FPGA EPCS 256 bytes 0x0 (default)
768-1023 (0x300 - 0x3FF)	WFM_GEN_DATA	R/W	23..0	256 samples of TEST pattern memory for fake data generator (must set registers 3 bits 7..0 and must set register 19 Bits (11..0) = odd channels Bits(23..12) = even channels