Top View

EP20K100TC144-2
clinkpc_pld

Top edge pins (144–109):

Pin	Signal
144	(VCC_IO)
143	|TXCLKIN (C,Column I/O)
142	|DAT2 (Column I/O)
141	|DAT1 (Column I/O)
140	|PWRDWN (Column I/O)
139	|RX0 (Column I/O)
138	|RX20 (Column I/O)
137	|RX19 (Column I/O)
136	|RX18 (Column I/O)
135	|RX17 (Column I/O)
134	(GND_IO)
133	|RX16 (Column I/O)
132	|RX15 (Column I/O)
131	|RX14 (Column I/O)
130	|RX13 (Column I/O)
129	(TRST)
128	(nCEO)
127	|CLK'0 (Dedicated Input, FAST')
126	(GND_INT)
125	(VCC_INT)
124	|CLK03 (Dedicated Input, FAST2)
123	(TDO)
122	|RX12 (Column I/O)
121	|RX11 (Column I/O, INT_DONE)
120	|RX10 (Column I/O, RDYnBSY)
119	|RX9 (Column I/O, CLKUSR)
118	|RX8 (Column I/O)
117	|RX7 (Column I/O, DAT'A1)
116	(VCC_IO)
115	|RX6 (Column I/O, DAT'A2)
114	|RX5 (Column I/O)
113	|RX4 (Column I/O, DAT'A3)
112	|RX3 (Column I/O, DAT'A4)
111	|RX2 (Column I/O, DAT'A4)
110	|RX1 (Column I/O)
109	|TX20 (Column I/O, DATA5)

Left edge pins (1–36):

Pin	Signal
1	(VCC_INT)
2	|TP6 (Row I/O)
3	|SCLK (Row I/O)
4	(GND_INT)
5	|TP0 (Row I/O)
6	|TP1 (Row I/O)
7	|TP2 (Row I/O)
8	|TP3 (Row I/O)
9	|TP4 (Row I/O)
10	|TP5 (Row I/O)
11	|RESETDRV (Row I/O)
12	(GND_IO)
13	|SW7 (Row I/O)
14	|SW6 (Row I/O)
15	|SW5 (Row I/O)
16	(VCC_INT)
17	(GND_INT)
18	(MSEL0)
19	(MSEL1)
20	|CLK40 (Dedicated Clock, CLK1)
21	(VCC_INT)
22	(NCONFIG)
23	|SW4 (Row I/O)
24	|SW3 (Row I/O)
25	|SW2 (Row I/O)
26	|SW1 (Row I/O)
27	|SW0 (Row I/O)
28	(VCC_IO)
29	|IO16 (Row I/O)
30	|DIR (Row I/O)
31	|CIOW (Row I/O)
32	|CIOR (Row I/O)
33	|CAEN (Row I/O)
34	(GND_INT)
35	|BUFEN (Row I/O)
36	(VCC_INT)

Bottom edge pins (37–72):

Pin	Signal
37	|A0 (Column I/O)
38	|A1 (Column I/O)
39	|A2 (Column I/O)
40	|A3 (Column I/O)
41	|A4 (Column I/O)
42	(GND_IO)
43	|A5 (Column I/O)
44	|A6 (Column I/O)
45	|A7 (Column I/O)
46	|A8 (Column I/O)
47	|A9 (Column I/O)
48	|D0 (Column I/O)
49	|D1 (Column I/O)
50	|D2 (Column I/O)
51	(TMS)
52	(TCK)
53	(D'edicated Input, FAST3)
54	(GND_INT)
55	(VCC_INT)
56	(D'edicated Input, FAST4)
57	|NSTATUS)
58	|CONF_DONE)
59	|D3 (Column I/O)
60	|D4 (Column I/O)
61	(VCC_IO)
62	|D5 (Column I/O)
63	|D6 (Column I/O)
64	|D7 (Column I/O)
65	|D8 (Column I/O)
66	|D9 (Column I/O)
67	|D10 (Column I/O)
68	|D11 (Column I/O)
69	|D12 (Column I/O)
70	|D13 (Column I/O)
71	|D14 (Column I/O)
72	(GND_IO)

Right edge pins (108–73):

Pin	Signal
108	(VCC_INT)
107	|TX0 (Row I/O)
106	(GND_IO)
105	|TX1 (Row I/O, DATA6)
104	|TX2 (Row I/O, DATA7)
103	|TX3 (Row I/O, nWS)
102	|TX4 (Row I/O, nRS)
101	|TX5 (Row I/O, nCS)
100	|TX6 (Row I/O)
99	|TX7 (Row I/O)
98	|TX8 (Row I/O, CS)
97	|TX9 (Row I/O, DEV_CLRn)
96	|TX10 (Row I/O)
95	|TX11 (Row I/O)
94	(DATA0)
93	(DCLK)
92	|RXCLKOUT (Dedicated Clock, CLK2)
91	(nCE)
90	(TDI)
89	(VCC_IO)
88	(GND_PLL)
87	(GND_INT)
86	(VCC_INT)
85	(VCC_PLL)
84	|TX12 (Row I/O, DEV_OE)
83	|TX13 (Row I/O)
82	|TX14 (Row I/O)
81	|TX15 (Row I/O)
80	|TX16 (Row I/O, LOCK)
79	|TX17 (Row I/O)
78	|TX18 (Row I/O)
77	(GND_INT)
76	|TX19 (Row I/O)
75	|D15 (Row I/O)
74	(GND_INT)
73	(VCC_INT)