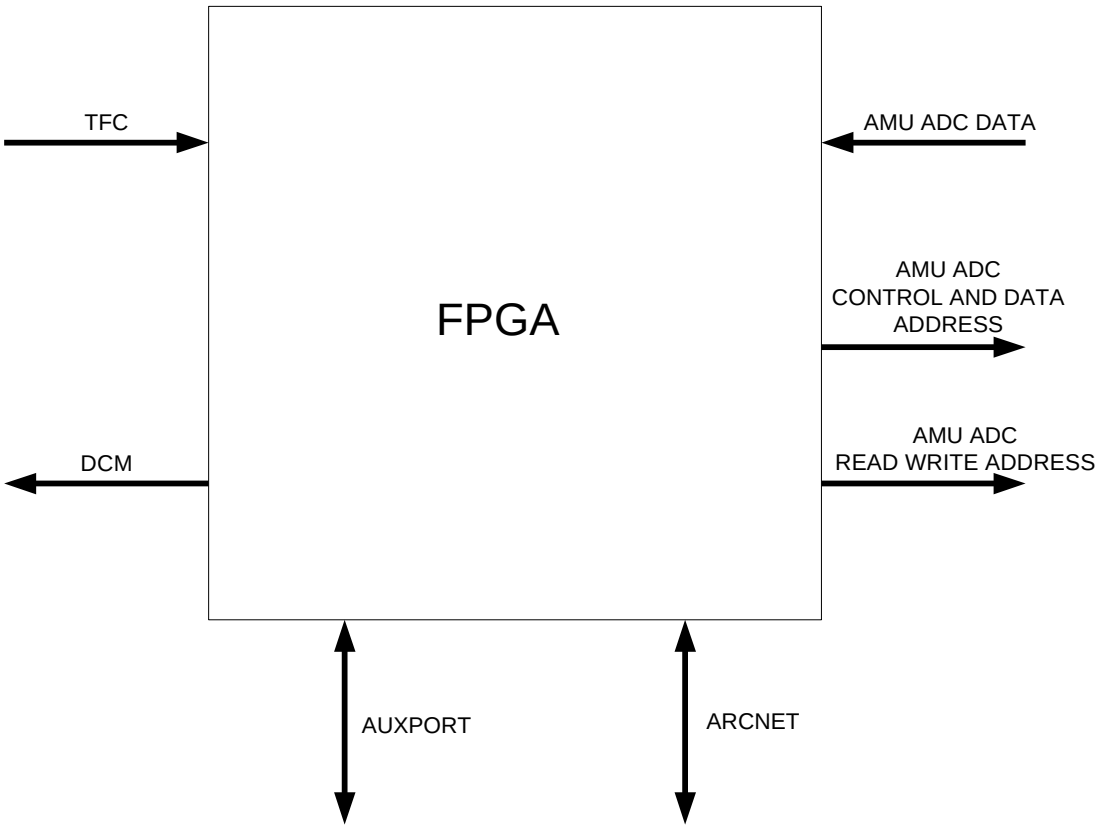
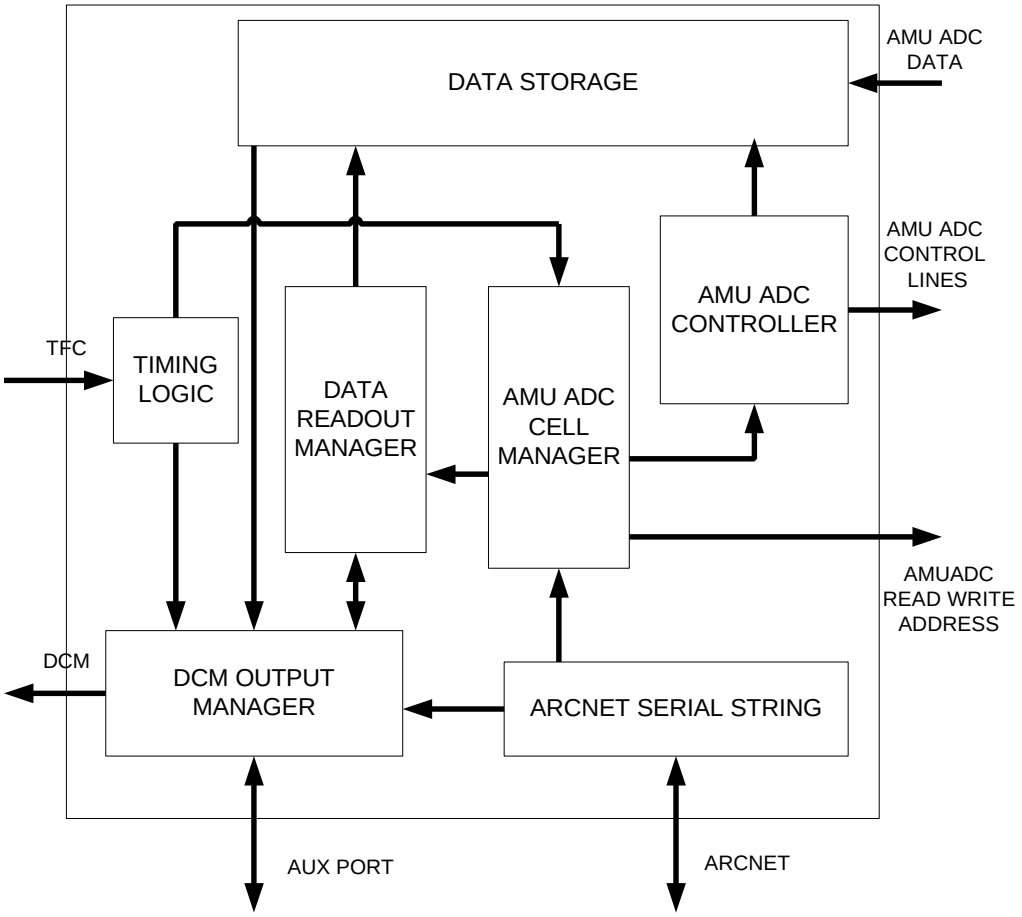
MUON TRACKER
CNTL FPGA



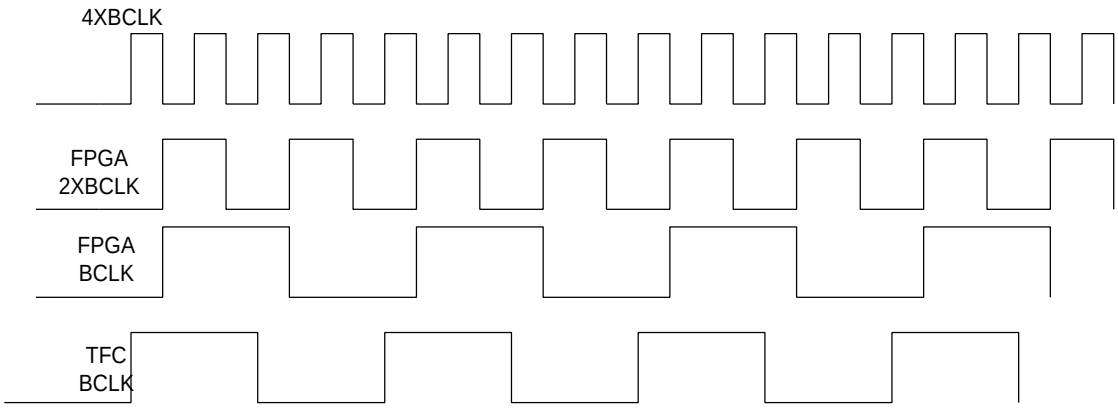


This document will discus the major blocks of the Muon tracker FPGA code and there interactions with each other.

The blocks that will be discussed are

- TIMING LOGIC
- AMU ADC CELL MANAGER
- AMU ADC CONTROLLER
- DATA STORAGE
- READOUT MANAGER
- DCM OUTPUT MANAGER

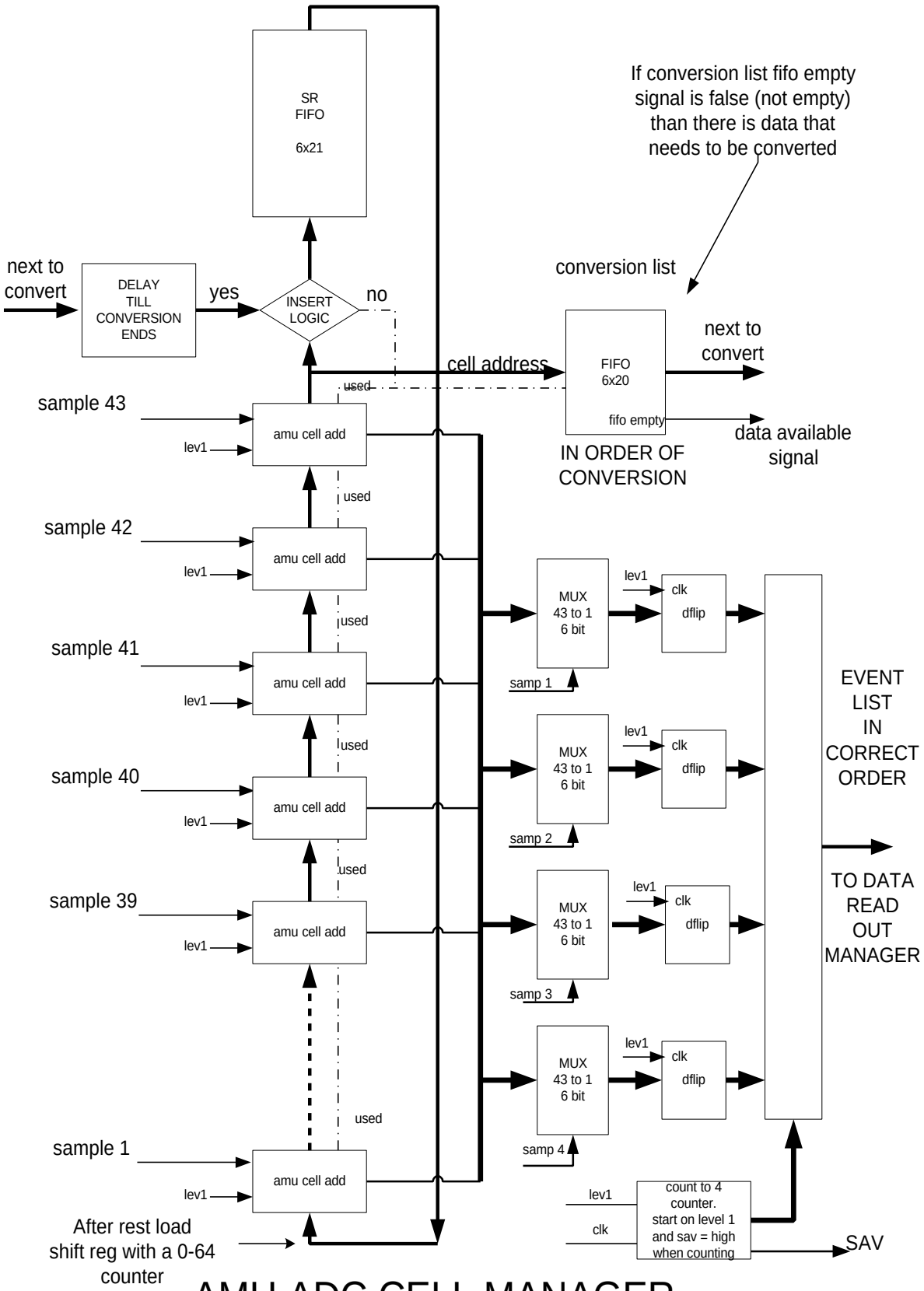
TIMING LOGIC



TIMING AND FAST CONTROL SINGNALS USED IN THE FPGA ARE
TFC CLK , BEAM CLK, LEVEL 1, MODEBIT ENABLE, ENDAT0 AND ENDAT1

IT TAKES 1 BEAM CLK FROM THE INPUT OF THE FPGA FOR THE LEVEL1 TO RECORD THE CELLS TO BE CONVERTED

All the Clock in The FPGA are derived from the four times beam clock on the GTM G-LINK. All the edges of the derived clocks are then adjusted to the rising edge of the real GTM beam clock . (this is done on a FPGA RESET)



AMU ADC CELL MANAGER

(A AMU ADC cell address is a pointer to a sample)

When a LEVEL 1 is received the MUON TRACKER would like to take 4 samples of data to best represent the event. Since the Level 1 occurs about 40 beam clocks after the event occurred some sort of scheme is required to handle the delay for recoding data. Not only is there a delay but samples can be spread out over a few beam clocks and with a possibility of Level 1 occurring every four beam clocks (limit 5) the same and overlapping cells can be used for multiple events.

These are some of the problems that are solved

- Once a cell is selected it must not be used till the is data stored.
- 40 beam clock delay
- The cells must always be written in numerical order
- Overlapping cells
- Same cells used in multiple events
- Handling the level 1 dead for four.
- Having this fit in the FPGA

AMU ADC CELL MANAGER DESCRIPTION

After a reset occurs the Cell manager starts loading its shift register and FIFO with data from a counter. It is completed after 67 beam clocks. After it is completed the FIFO is loaded with the cells 0-20 and the shift register is loaded with 21 to 63. every beam clock data is popped from the FIFO and clocked in the shift register so that there is a closed loop.

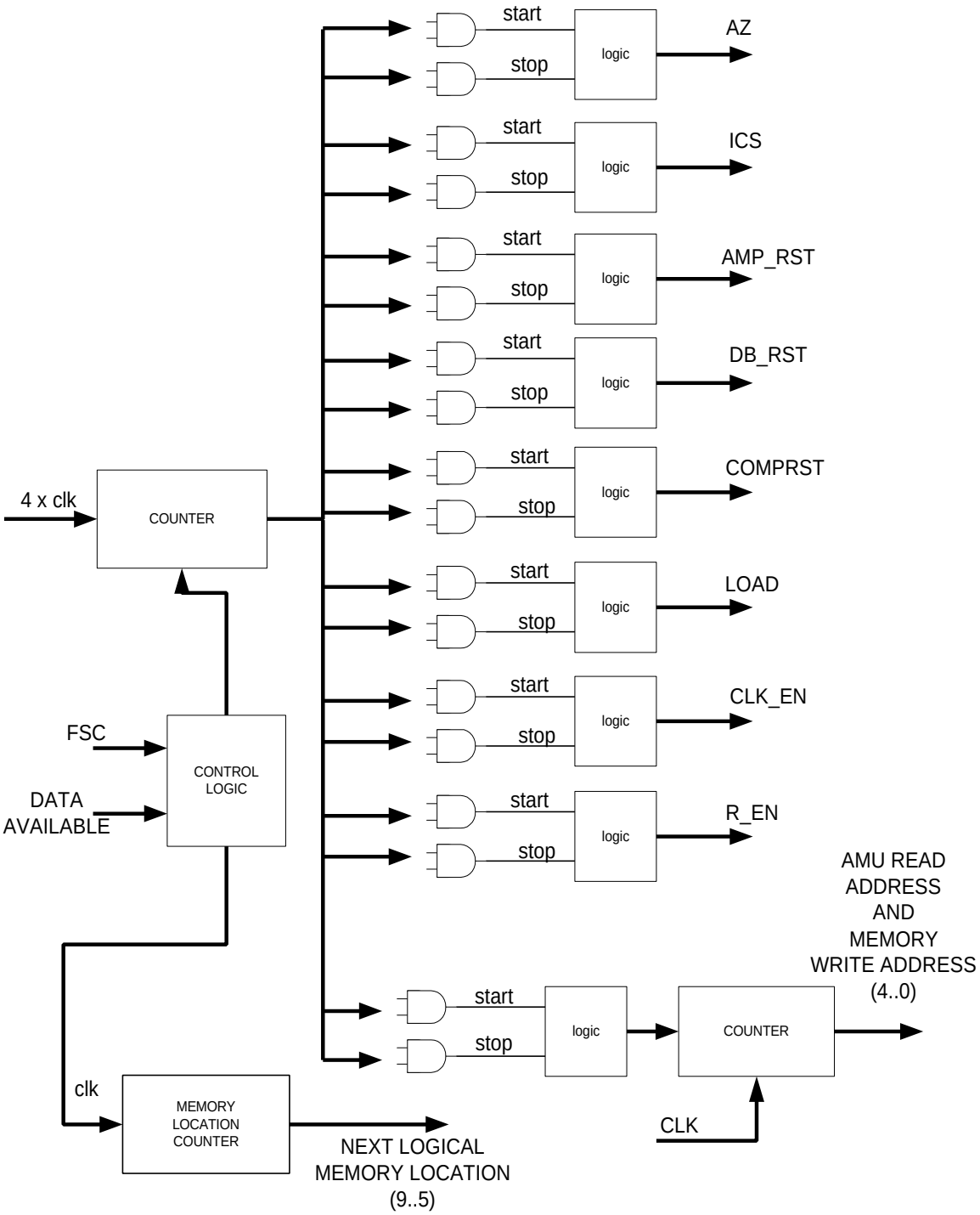
When a level 1 occurs the sample input to each register is clocked into a used bit. (only 4 sample lines are selected to indicated which 4 cells to be used) at the same time there are four 43 to 1 mux's which are set to the same cells in the sample lines and the output of the muxs are clocked into a filp flop. So after a level1 four use bits are set high and the sample cells are located in the four flip flops. After each clock the samples stored in the flip flops are clocked out to the event list. The use bits follow the cells up the shift register till it reaches the insert logic. If the cell was used in an event it will NOT be clocked into the SR FIFO; it will be clocked into the conversion FIFO.

There are two lists generated by the AMU CELL manager the event list and the conversion list. The event list contains the cells used for each event in the correct order. The conversion list has the cells in numerical order and it is the order of conversion.

The event list is used by the DCM OUPUT manager to let the real world know what cells were used for that event. It is also used in the readout manager to find the address of the data stored in the dual port memory.

The conversion list is used by the AMU ADC CONTROLLER to start a conversion on the correct cell and is used to put back the cell in the cell manager cell loop.

The insert logic takes the cell from the conversion list after conversion and puts it in the list. (numerical order)



AMU ADC CONTROLLER

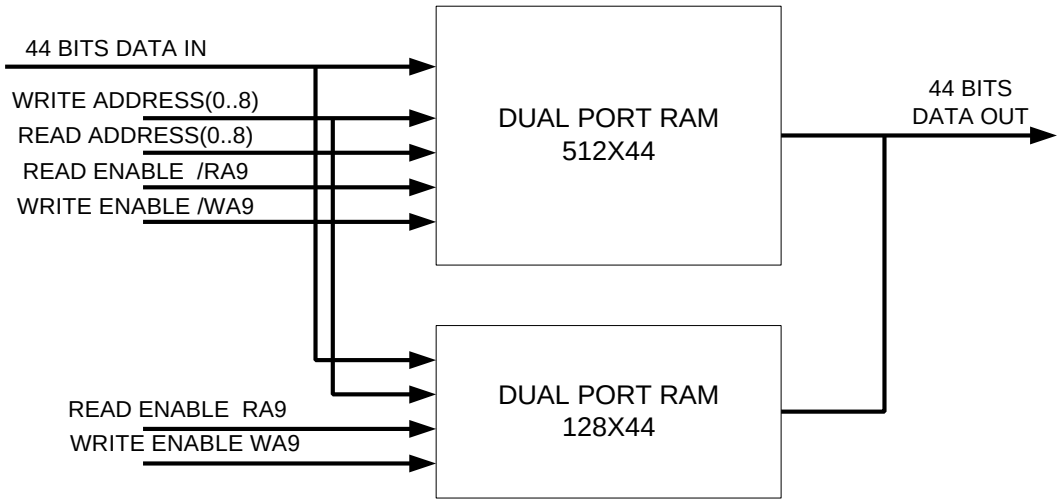
The AMU ADC CONTROLLER is started by the data available signal from the Cell Manager conversion FIFO or from the AMU ADC FULL SCALE COUNT (FSC). When it gets a signal it will start a counter and with simple logic generate the necessary signals to control the AMU ADC.

Every time the conversion finishes it increments the memory location counter to the next logical memory block (explained in data store). The ADDRESS used to read the data from the AMU ADC is also used in the DUAL PORT memory. So the logical address and the 5 bit AMU address make a complete address for the data block.

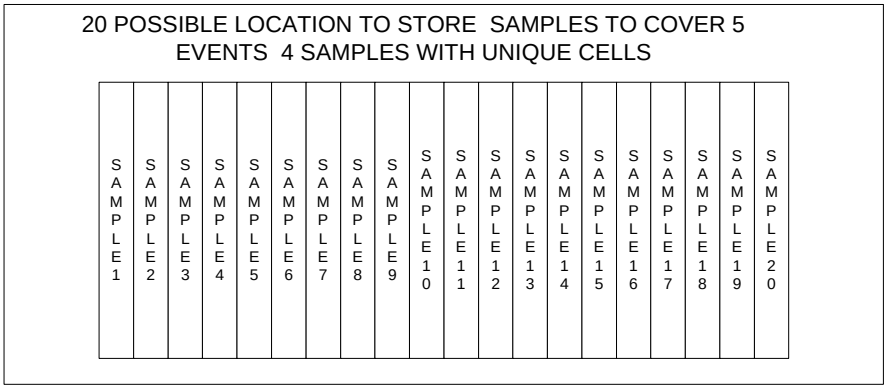
The FSC also triggers the conversion list FIFO to release the next cell to be converted. At the end of conversion the cell is put back in the CELL MANAGER LOOP.

The FSC is generated by or'ing all the four FSC from each AMU ADC. The result will be delayed by 3 beam clocks to start the conversion.

DATA STORAGE

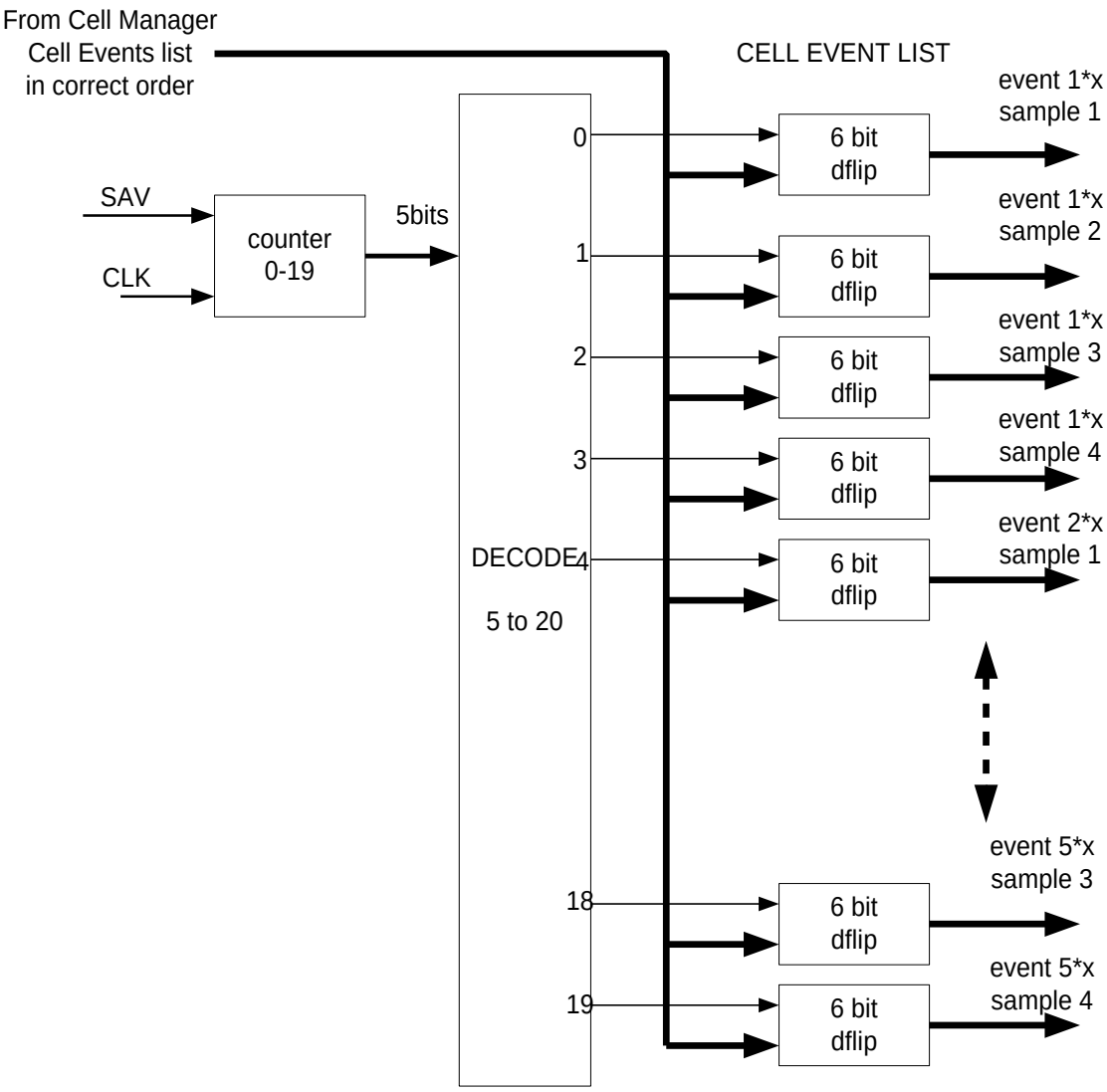


SIMPLIFIED MEMORY
BLOCK DIAGRAM



LOGICAL MEMORY
BREAK UP

The Data Storage is a dual port memory 640x44bits and is broken down in to 20 sample location (logical address 0 to 20). Each sample location is 32 words deep and 44 bits wide. And it is just enough memory to hold one sample from all four AMU ADCS. The benefit from breaking up the memory in terms of samples rather than events is that samples that are used in two events do not have to be duplicated. The Data Storage can now easily be loaded each sample at a time as the conversions take place without worry of what event get what sample. And the logical location is incremented for every new sample in the AMU ADC CONTROLLER.



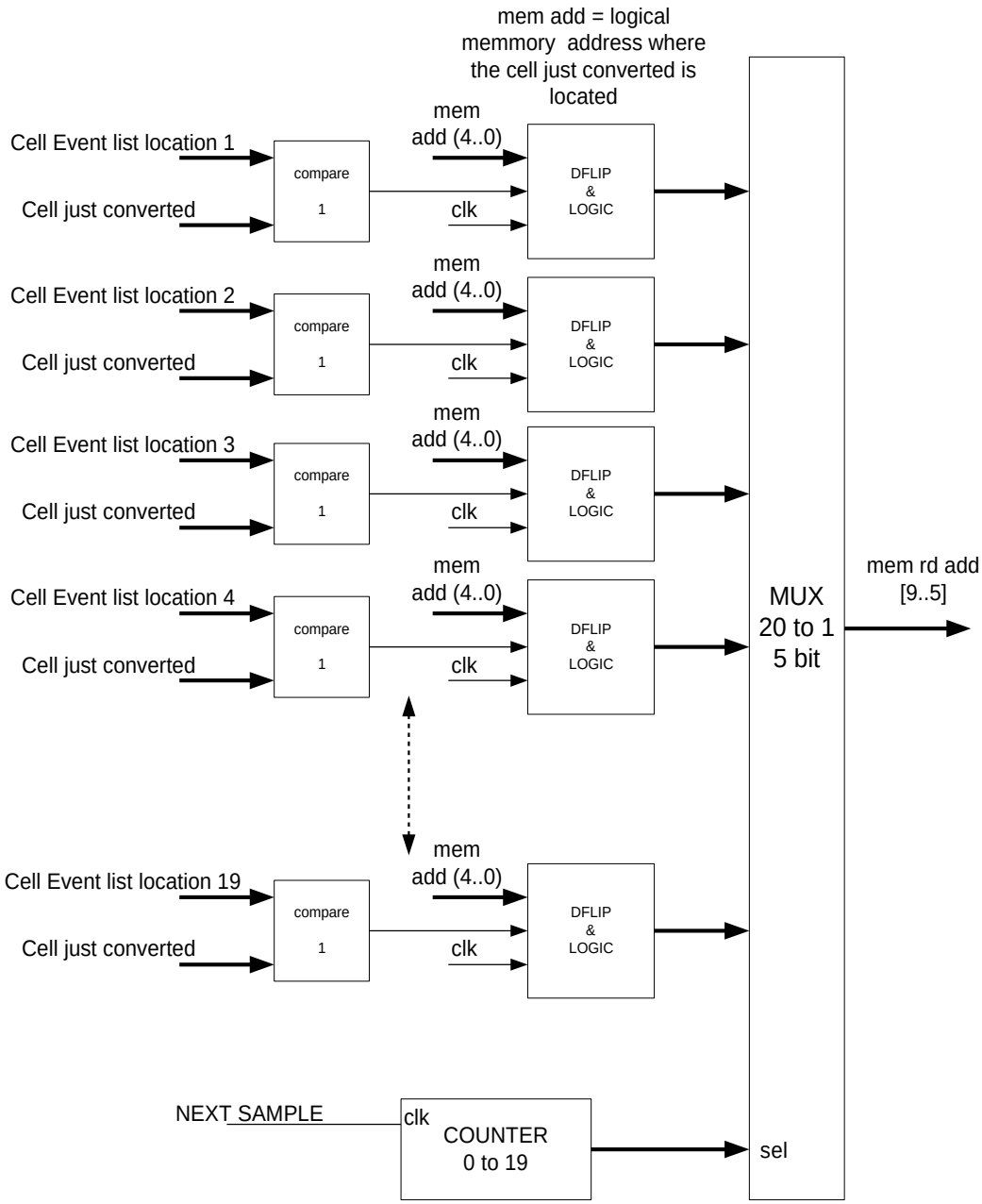
The ouptuts of this modulal list all the cells in the correct order from the last 5 event. (the order the samples must be read out to the DCM.)

0 1 2 3 = event 1 * X
4 5 6 7 = event 2 * X
8 9 10 11 = event 3 * X
12 13 14 15 = event 4 * X
16 17 18 19 = event 5 * X

where

X = 5 DIV number of of level1 :: to the highest integer

READ OUT MANAGER
PART 1

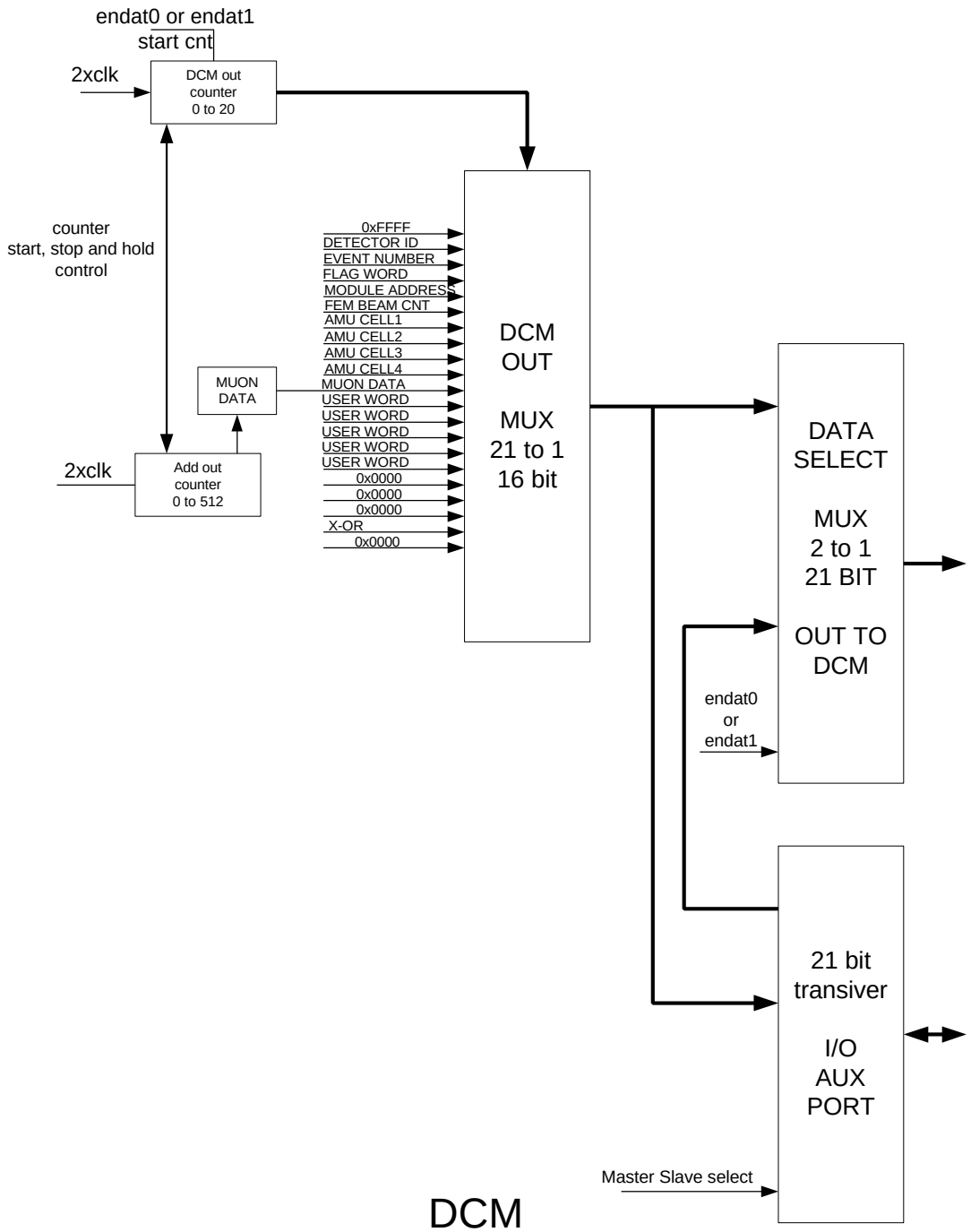


READ OUT MANAGER PART 2

The Read Out Manager Part one is really an extension of the Cell Manager. All it does is receive the data from the event list output and stores it in parallel flip flops so all the events and samples can be read out at once.

Read Out Manager Part 2 is slightly more complicated. It is responsible for finding the correct logical address for the next sample to be read out over the DCM.

The event list holds the cells in the correct order of events from event 1 to 5 and sample 1 to 4. After a conversion is completed by the AMU ADC Controller the Read Out Manager compares all the cells in the event list to the cell just converted. If the value matches then the logical address is then stored in the corresponding flip flop. All the logical addresses stored in the flip flops go into a large 20 to 1 ,5 bit mux . Since the logical address are now in order of events a simple 0 to 19 counter can be incremented for each of the next samples to be read out.



DCM
OUTPUT MANAGER

The DCM OUTPUT MANAGER is primarily controlled by the ARCNET serial string. The serial string by default loads the FPGA to respond to endat0 and to allow for endat1 to use the AUX port.

The Output manager is a large MUX with a counter selecting at each clk what to send over to the DCM. Looking at the diagram explains most of it except for the data read out which is also fairly simple. Once the counter reaches the data section, the MUX counter is stopped and waits for the data counter to reach 512. All data sent it then resumes till the end of count and waits for the next endat.

Things to KNOW..

- Both Endat1 and endat0 send data to the DCM output lines
- The endat1 signal from the GTM controles the MUX to select between AUX port or the DATA from FPGA
- The ARCNET serial string can mask endat1 or endat0
- The signal Bdsel on the ARCNET serial string controls which signal the FPGA will respond to ENDAT1 or ENDAT0
- The ARCNET serial string is used to load the user words for read out