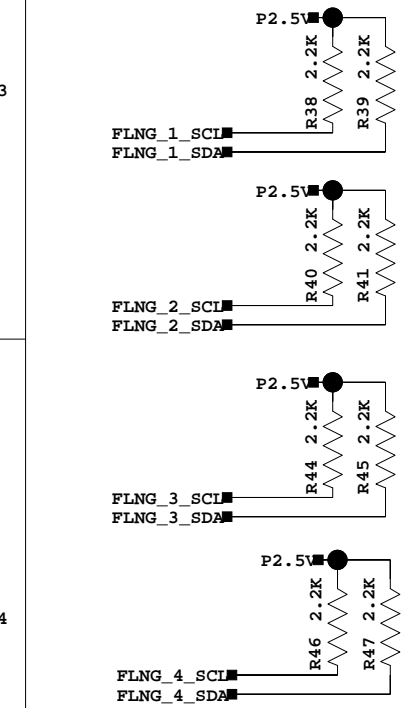
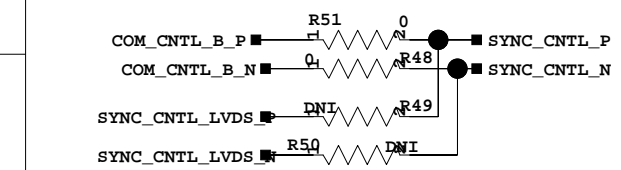
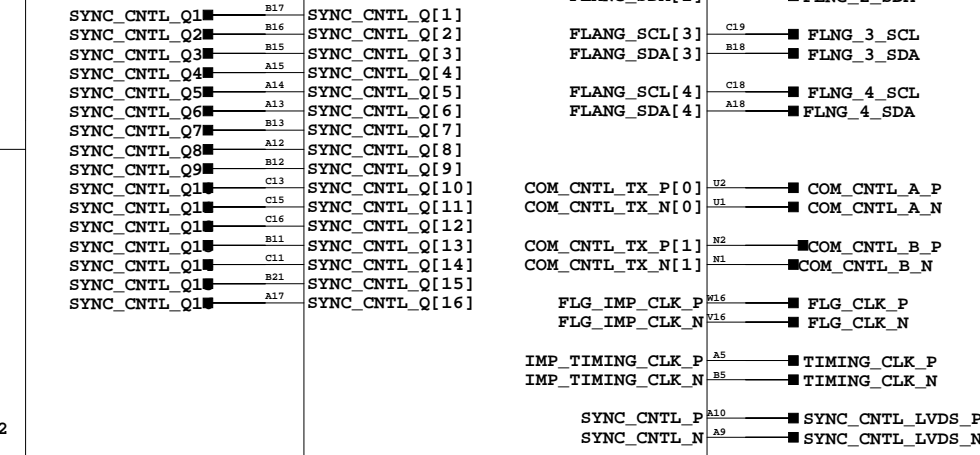
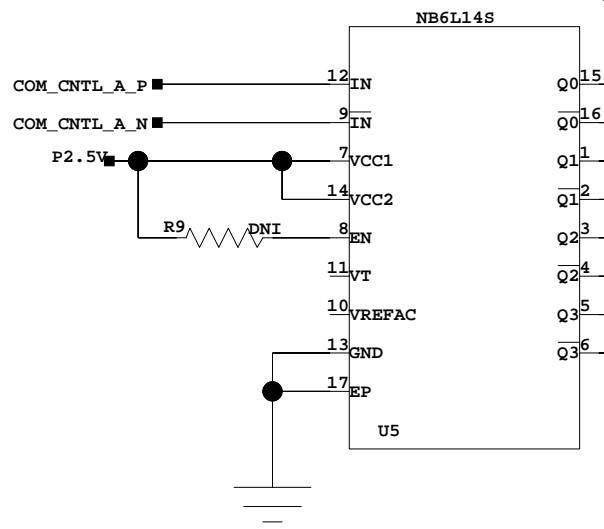


**MATCHED LENGTH
to 1/2 inch**

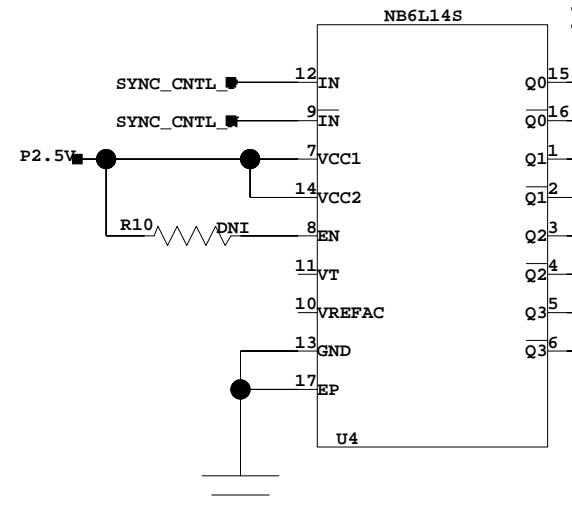


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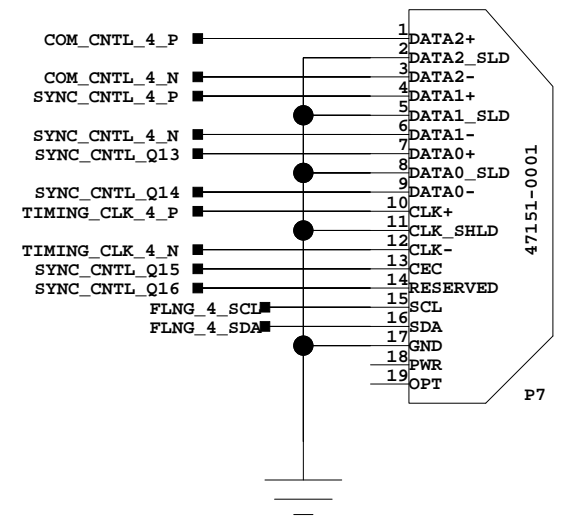
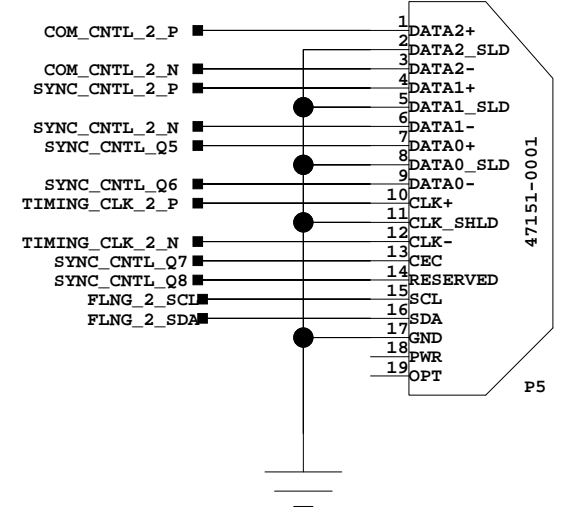
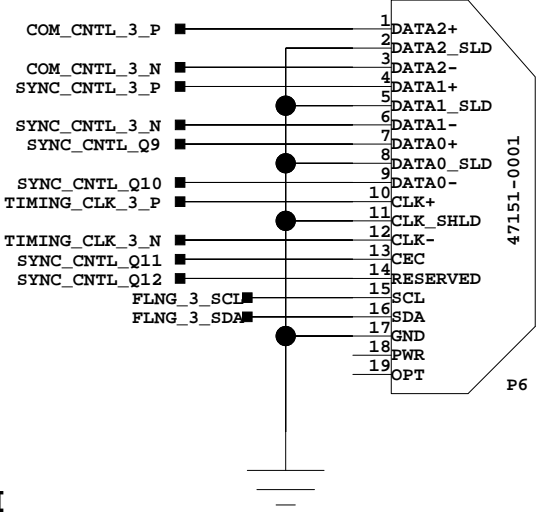
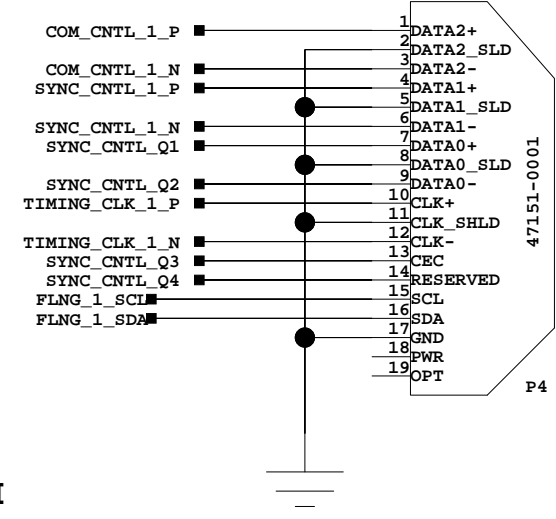
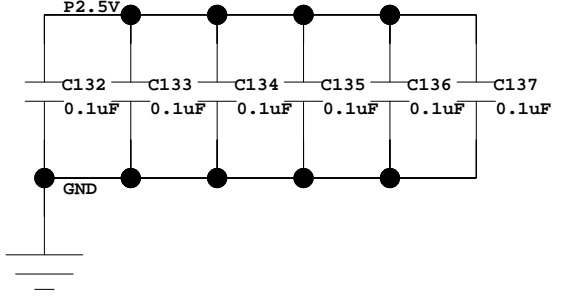
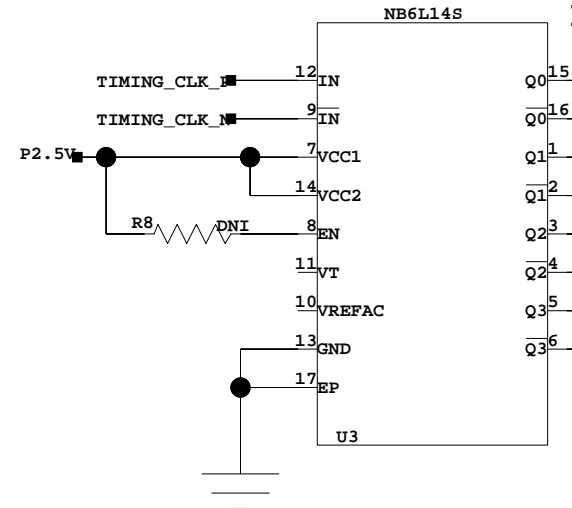
**MATCHED LENGTH
GROUP 1**



**MATCHED LENGTH
GROUP 2**



**MATCHED LENGTH
GROUP 3**

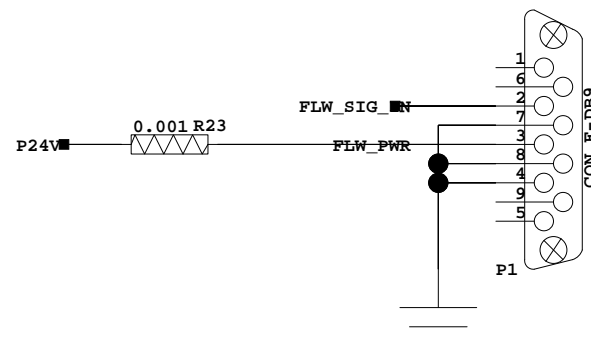
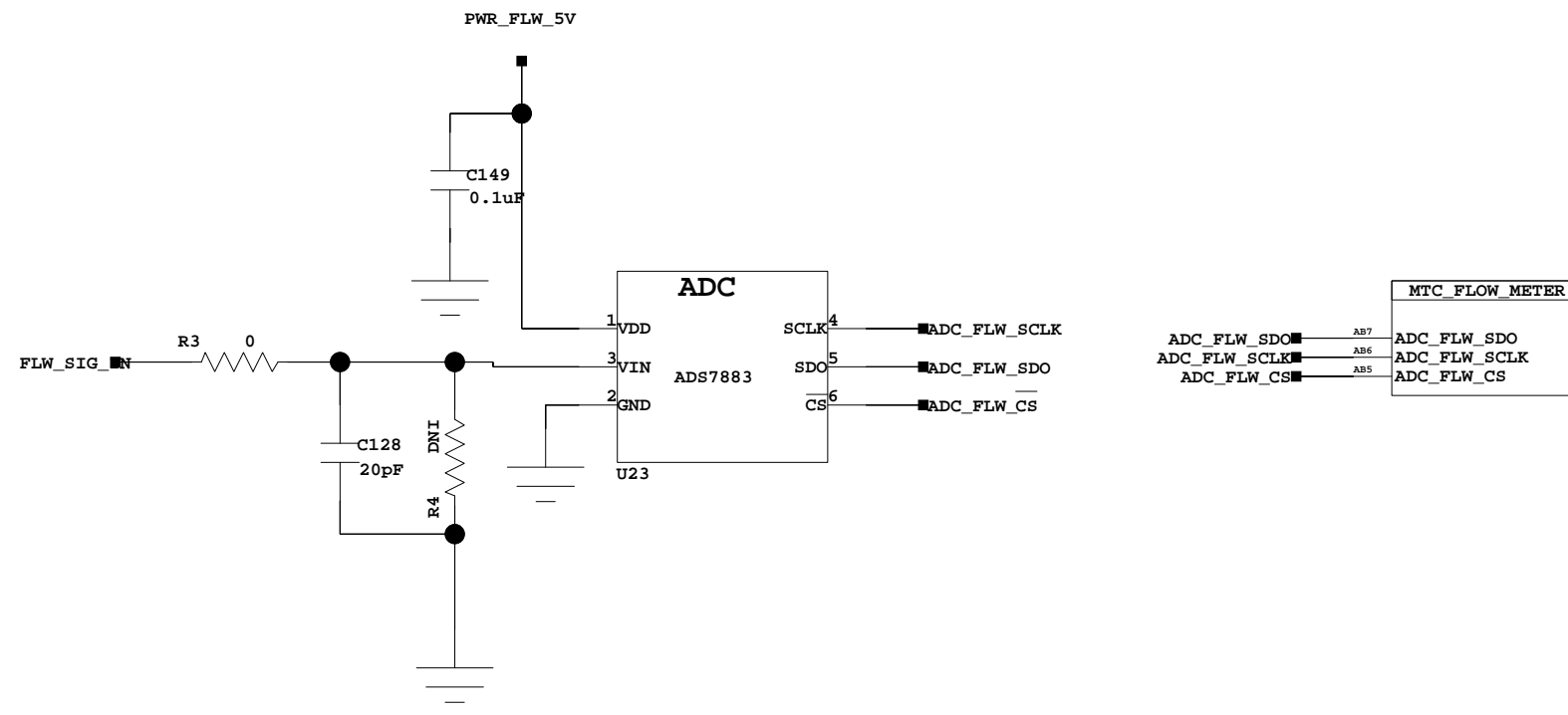
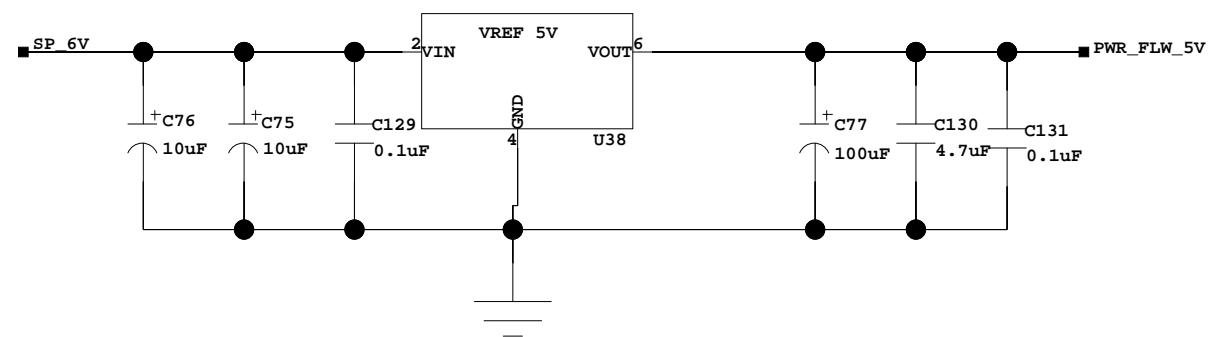


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MASTER TIMING CONTROL BOARD

TIMING_POWER_INPUT

Date: 28/06/2016:10:42 DRAWN BY: Jack Fried



GM50A001103RA3020 Mass Flow Meter,

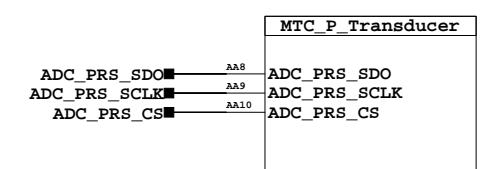
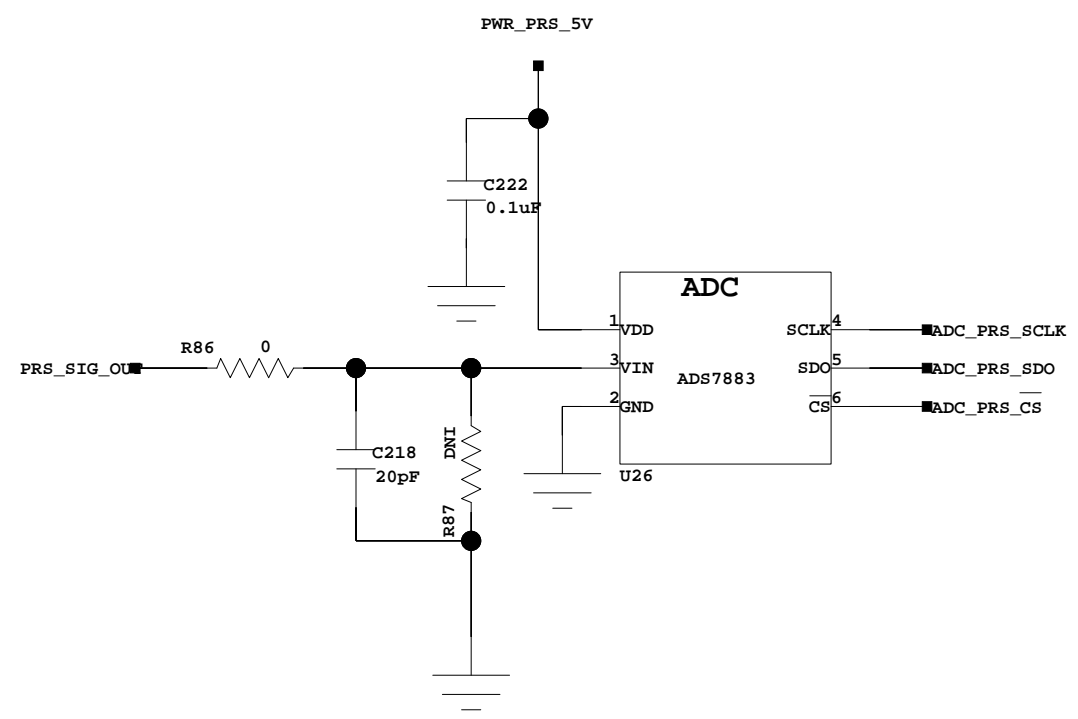
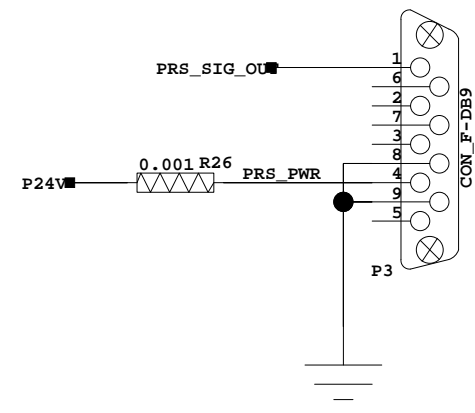
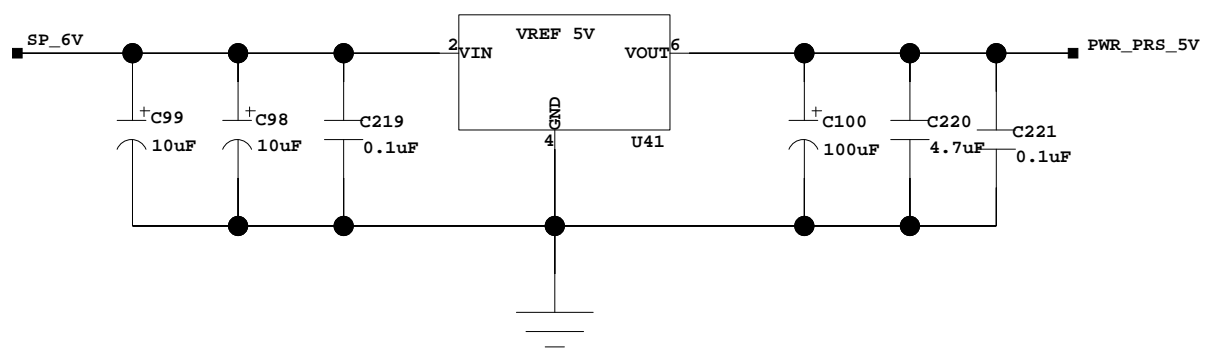
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 UPTON N.Y. 11973

MASTER TIMING CONTROL BOARD

Flow Meter

Date:
 28/06/2016:10:29

DRAWN BY:
 Jack Fried



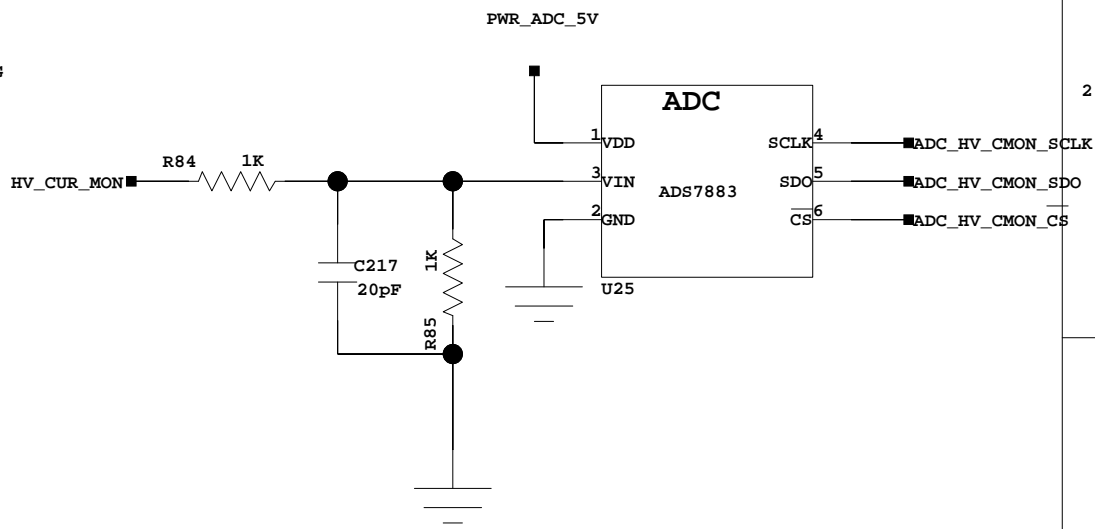
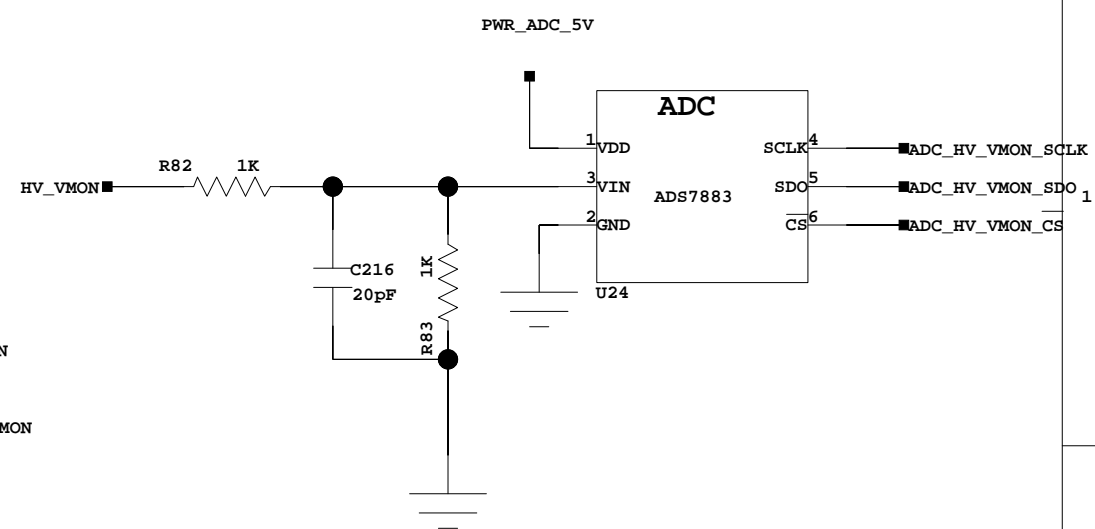
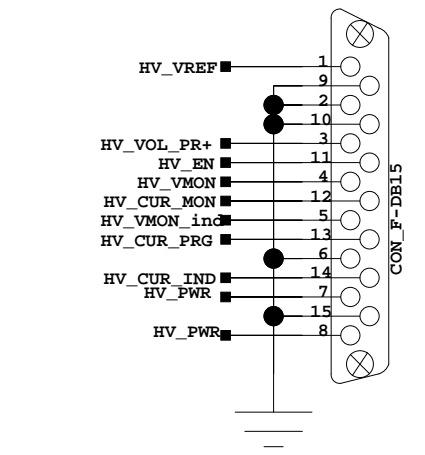
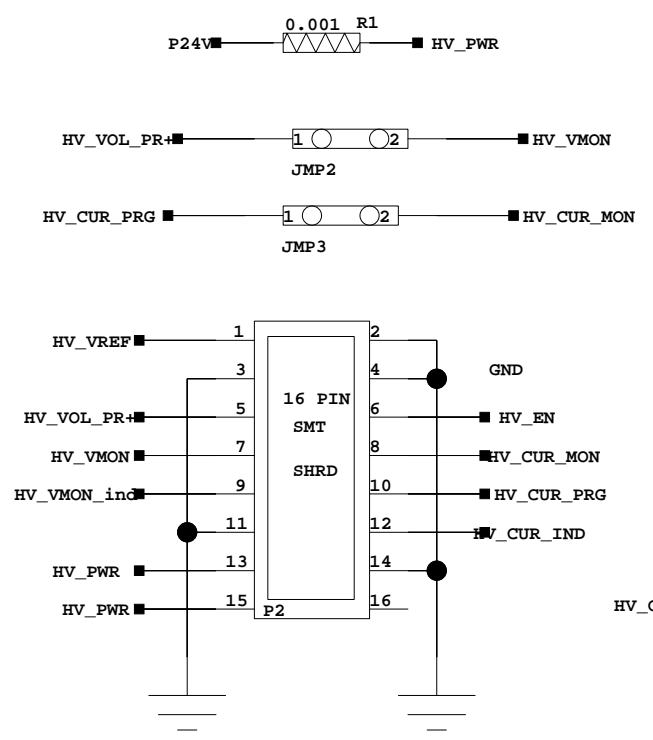
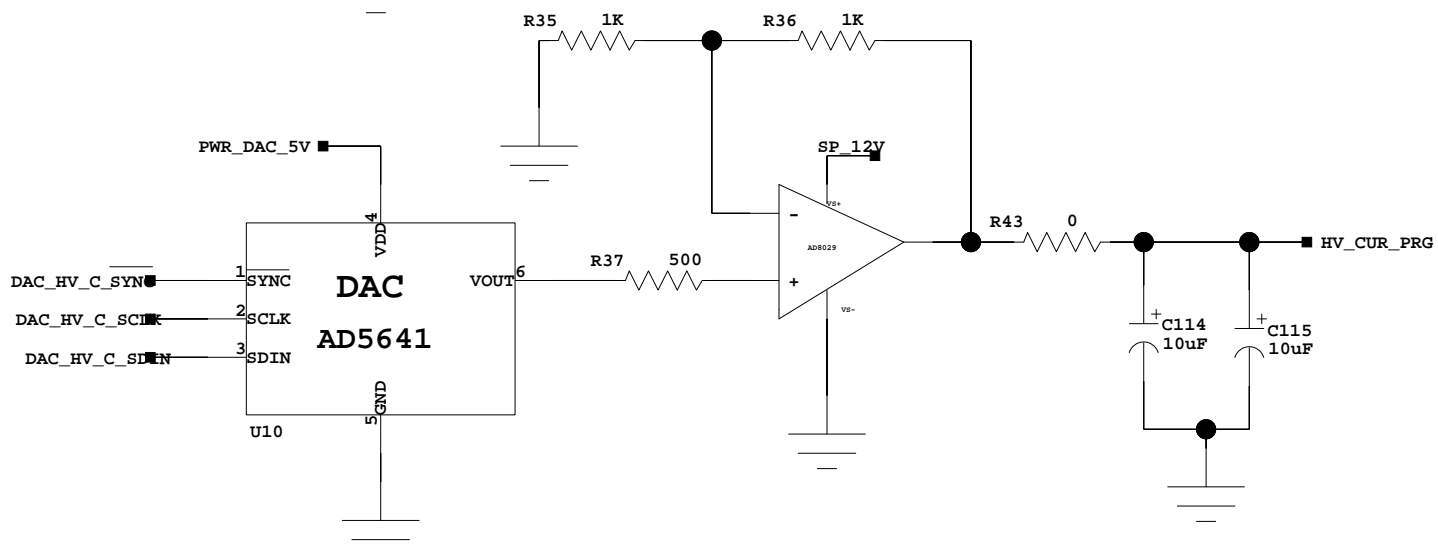
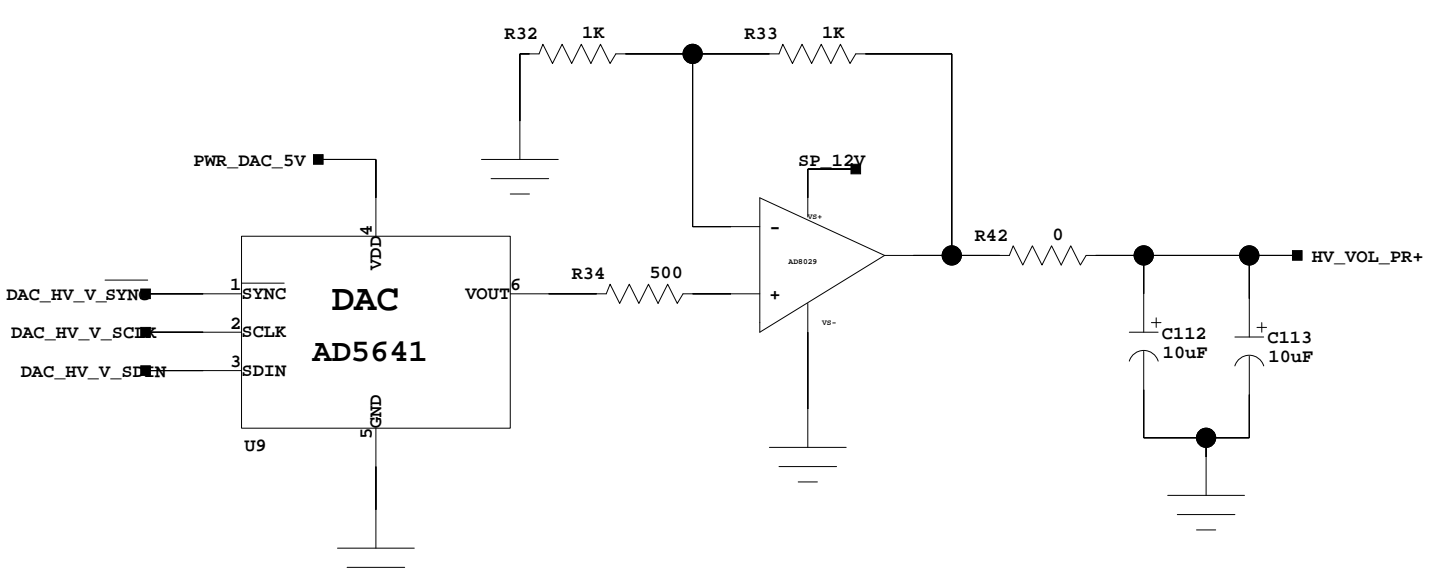
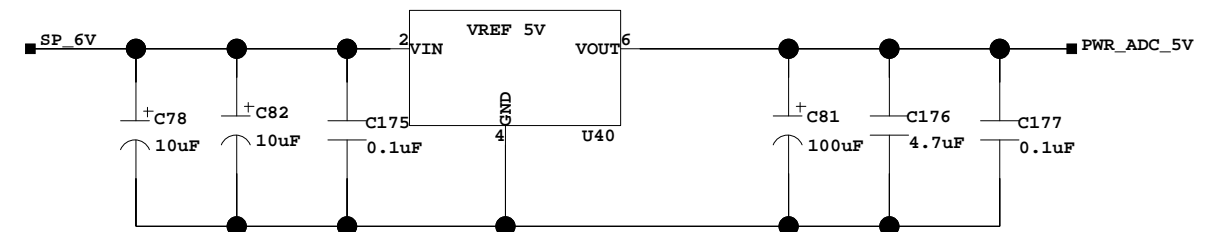
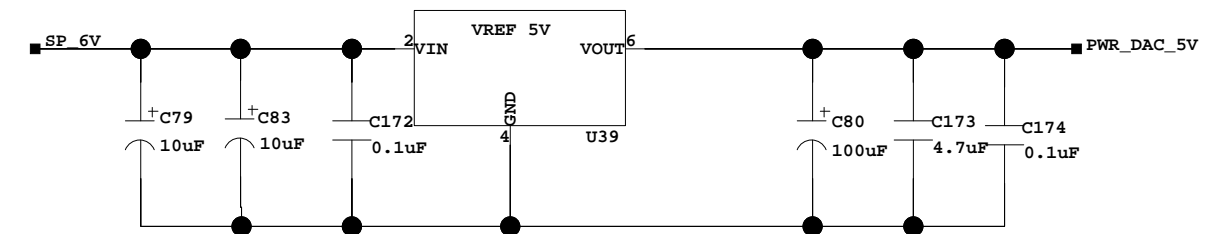
870 & 872 Pressure Transducer

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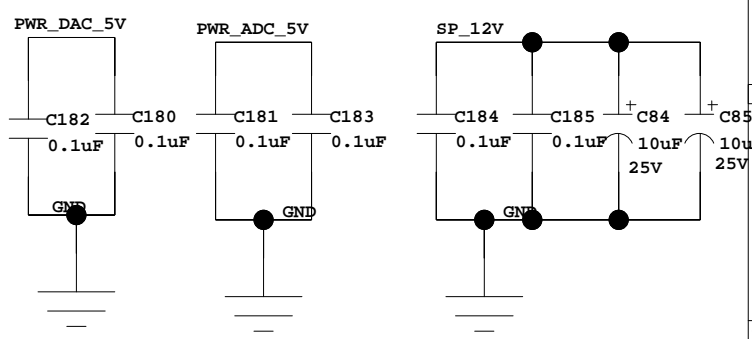
MASTER TIMING CONTROL BOARD Pressure Transducer

Date: 28/06/2016:10:29 DRAWN BY: Jack Fried

ULTRAVOLT HV



MTC_HIGH_VOLTAGE_CNTRL			
DAC_HV_C_SCLK	Y22	DAC_HV_C_SCLK	ADC_HV_VMON_SDO
DAC_HV_C_SDIN	AA19	DAC_HV_C_SDIN	ADC_HV_VMON_SCLK
DAC_HV_C_SYNC	AA18	DAC_HV_C_SYNC	ADC_HV_VMON_CS
DAC_HV_V_SCLK	AA20	DAC_HV_V_SCLK	ADC_HV_CMN_SDO
DAC_HV_V_SDIN	Y21	DAC_HV_V_SDIN	ADC_HV_CMN_SCLK
DAC_HV_V_SYNC	W22	DAC_HV_V_SYNC	ADC_HV_CMN_CS
			AB21
			AB20
			AB18
			AB17
			AA22
			AB22

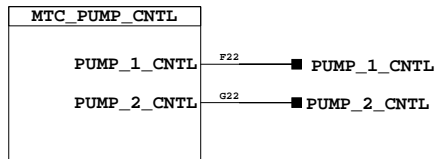
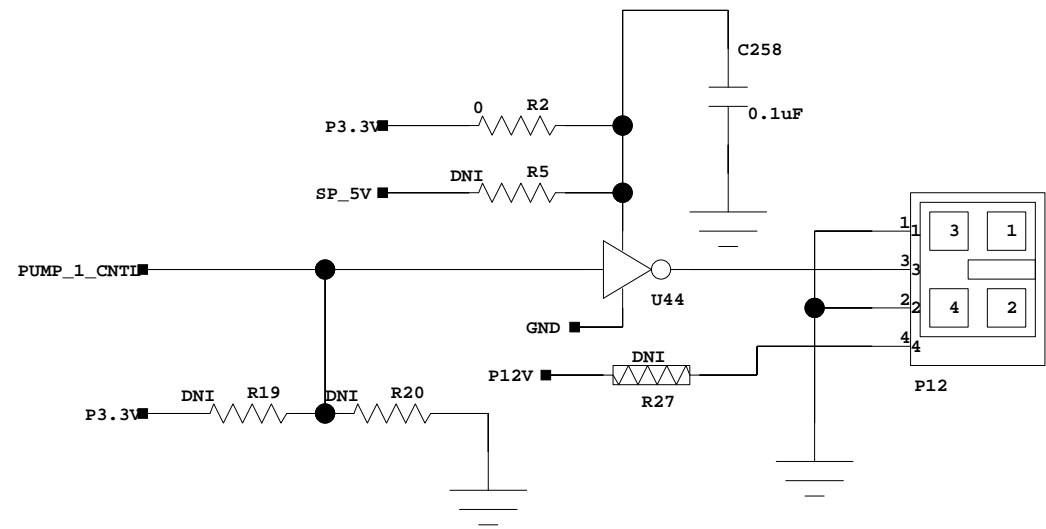


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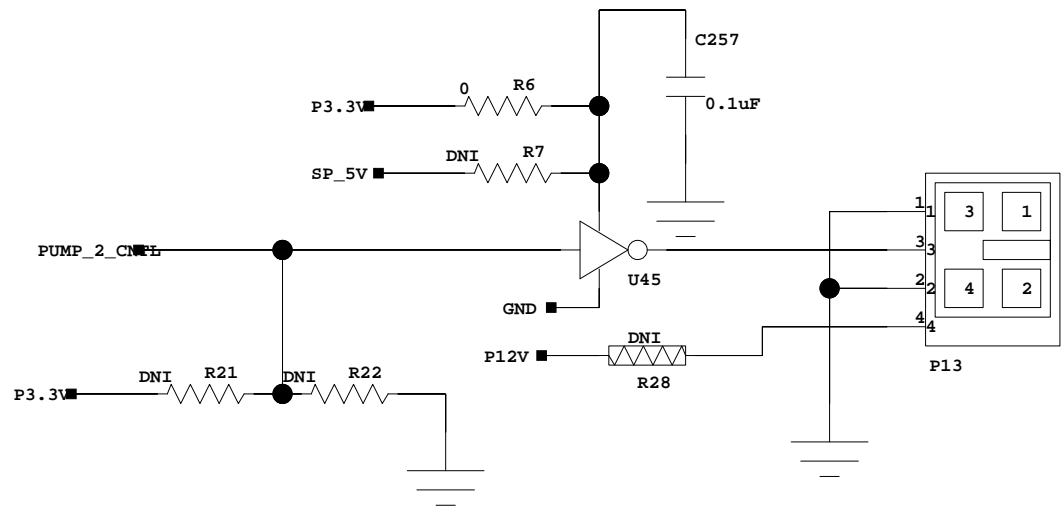
MASTER TIMING CONTROL BOARD High Voltage Control

Date: 28/06/2016:10:29
DRAWN BY: Jack Fried

PUMP 1 CONTROL



PUMP 2 CONTROL

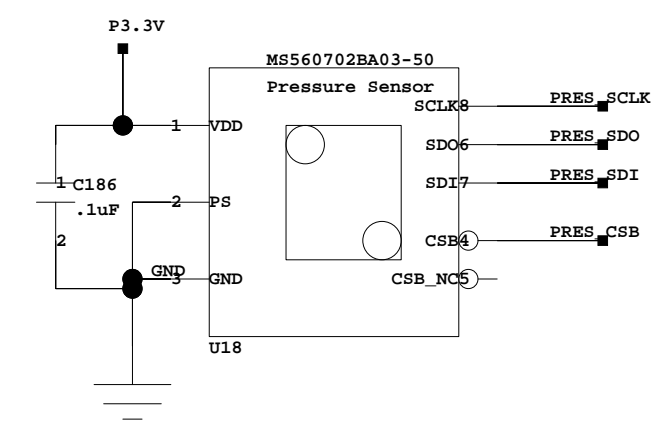
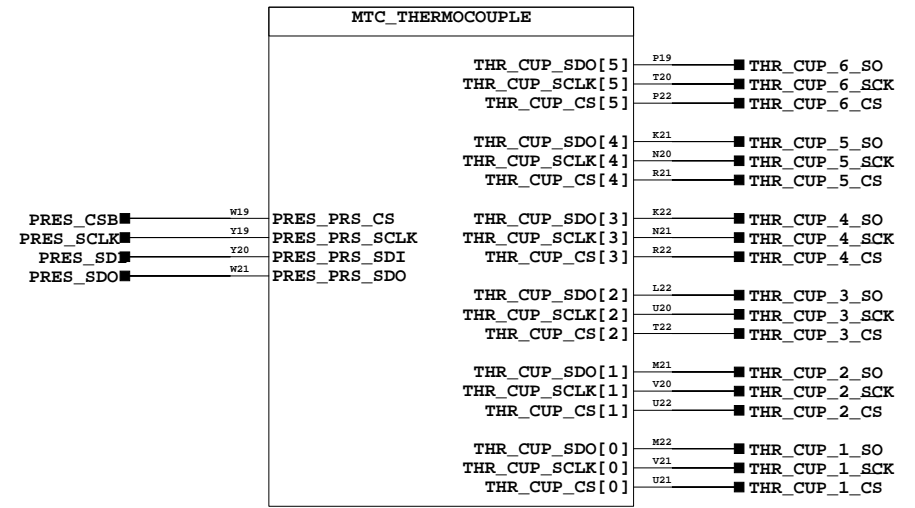
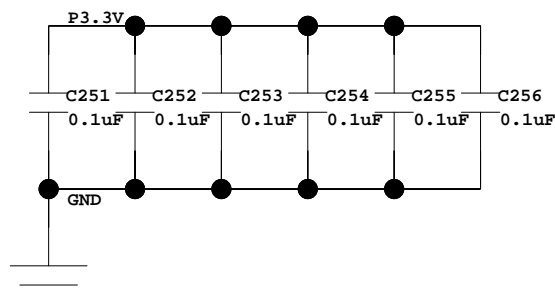
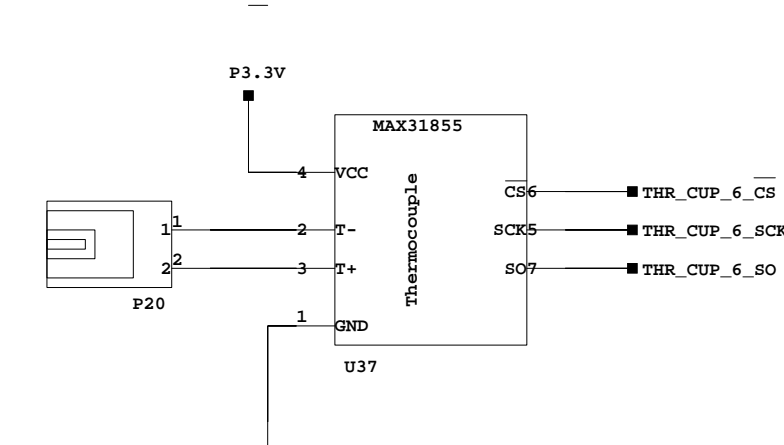
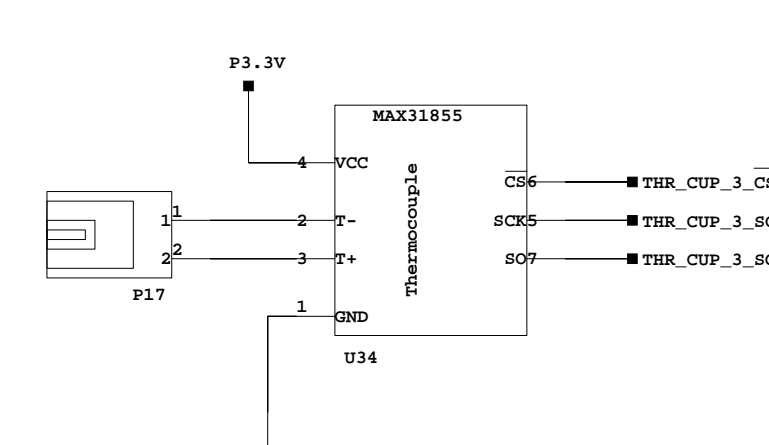
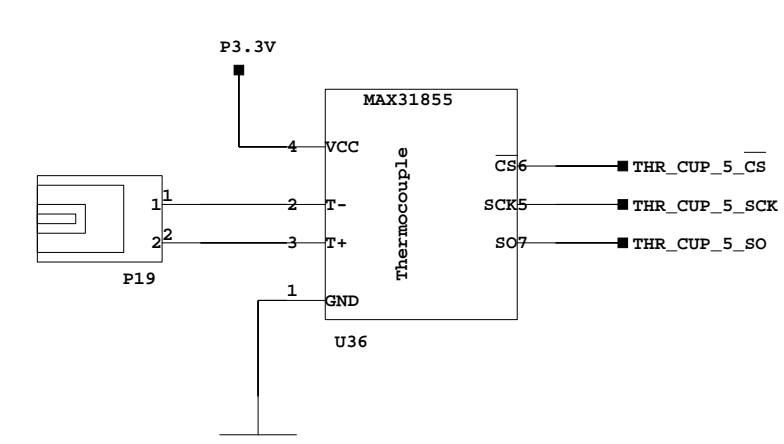
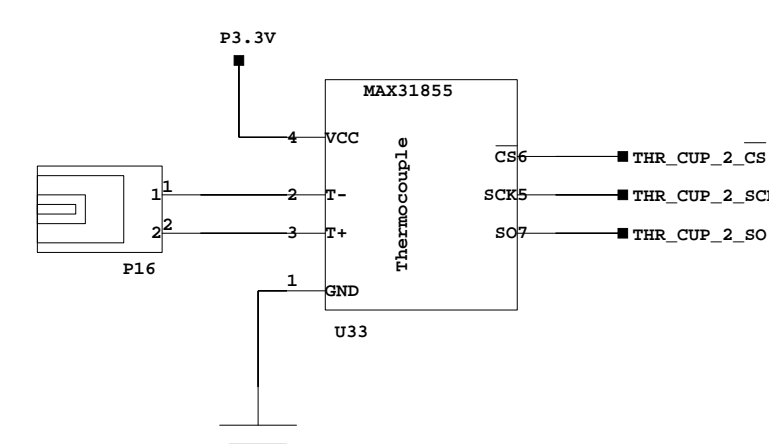
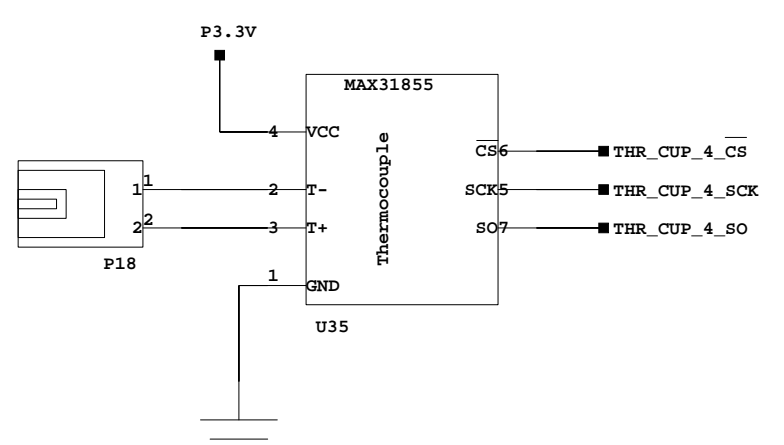
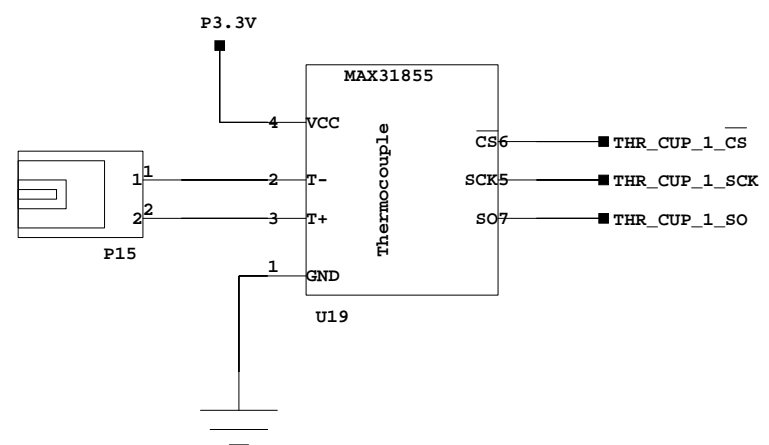


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MASTER TIMING CONTROL BOARD

Pump Controller

Date: 03/06/2016:12:30
 DRAWN BY: Jack Fried



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MASTER TIMING CONTROL BOARD
Temp and Pressure Sensor

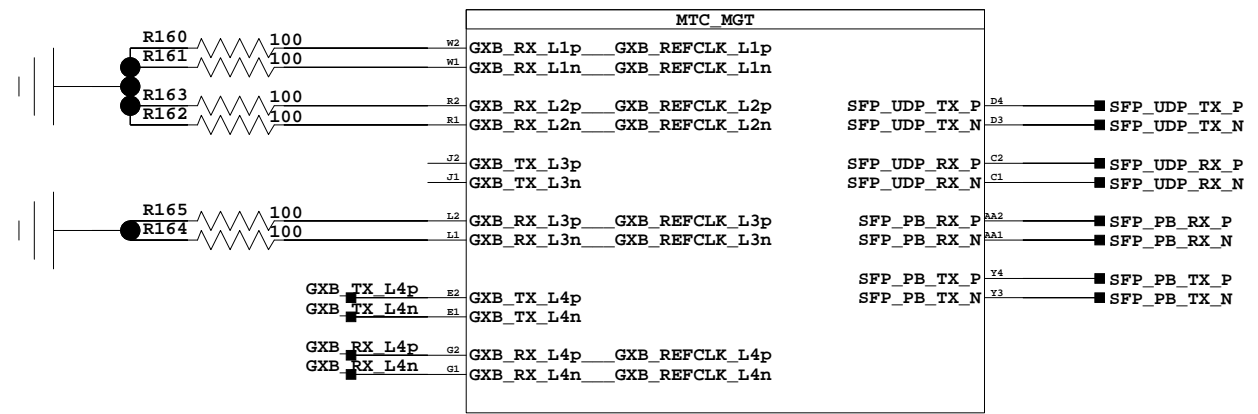
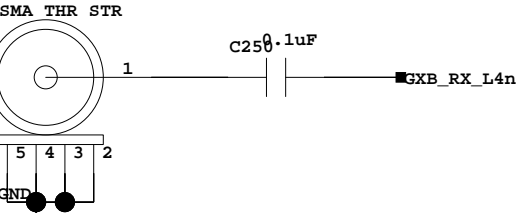
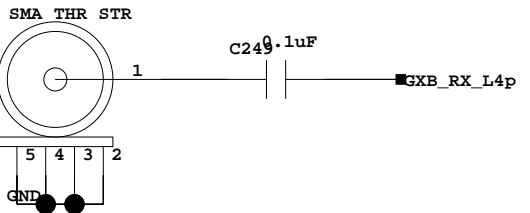
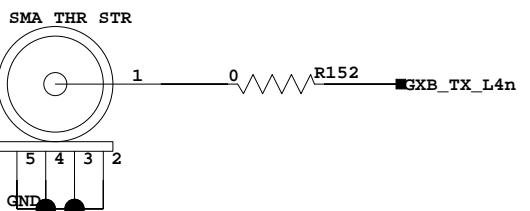
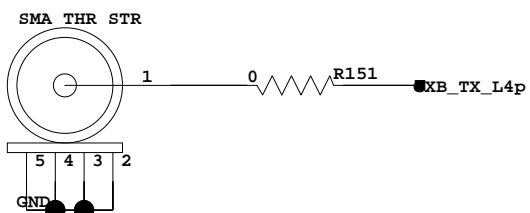
Date: 03/06/2016:12:33
 DRAWN BY: Jack Fried

A

B

C

D



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MASTER TIMING CONTROL BOARD
MTC FPGA MGT

Date:
25/05/2016:12:53

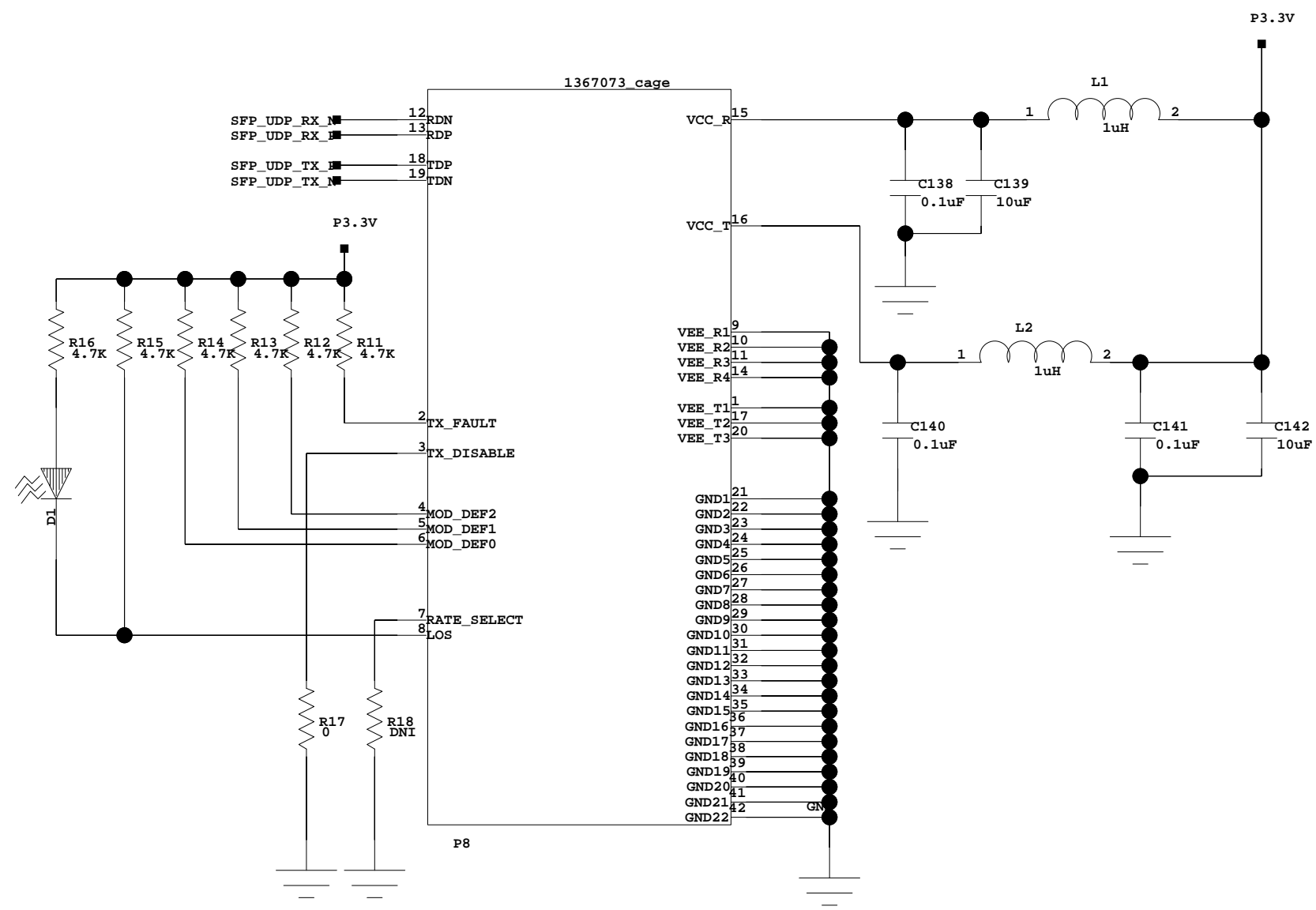
DRAWN BY:
Jack Fried

A

B

C

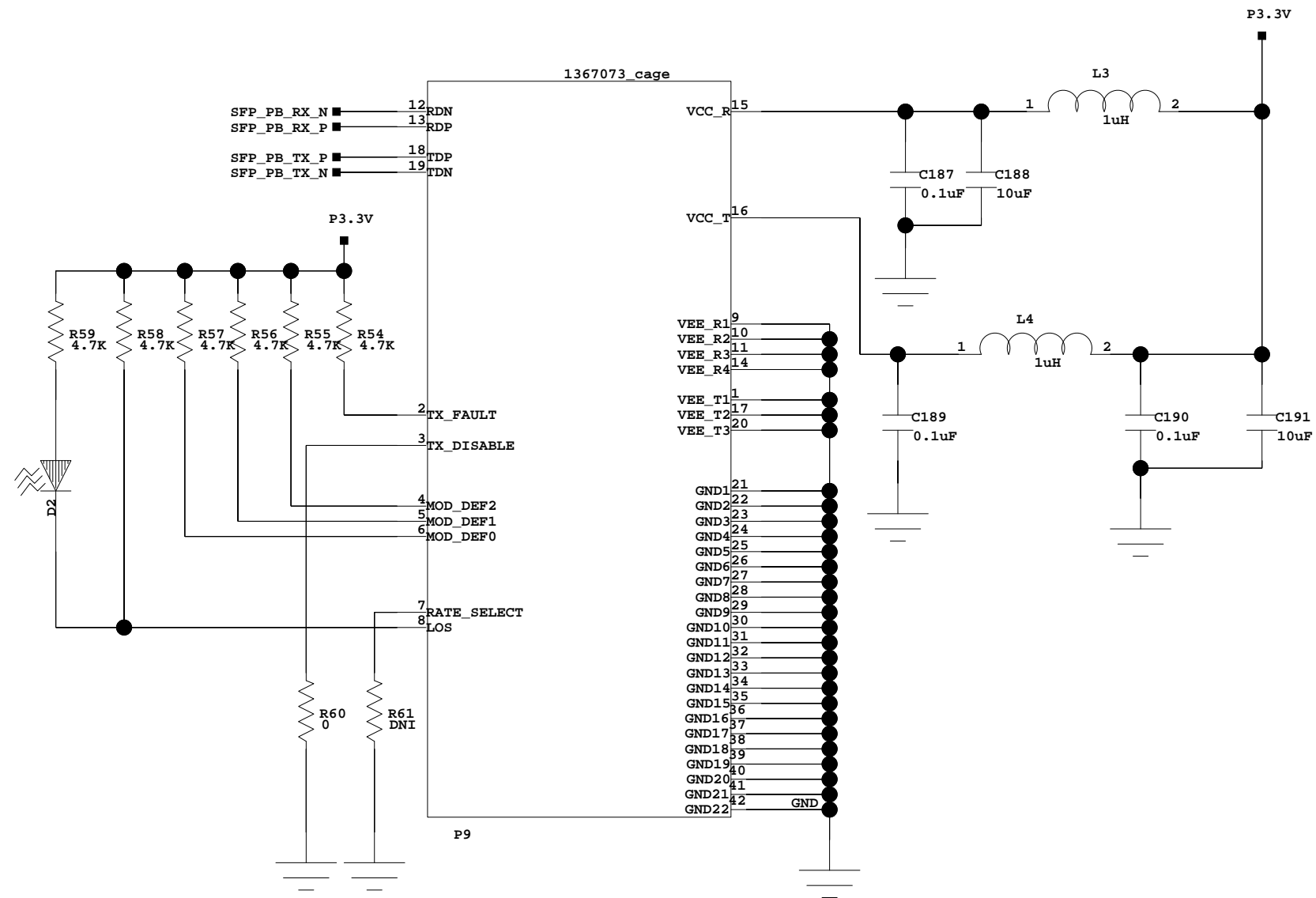
D



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MASTER TIMING CONTROL BOARD
Gigabit Ethernet SFP

Date: 24/05/2016:12:57
 DRAWN BY: Jack Fried

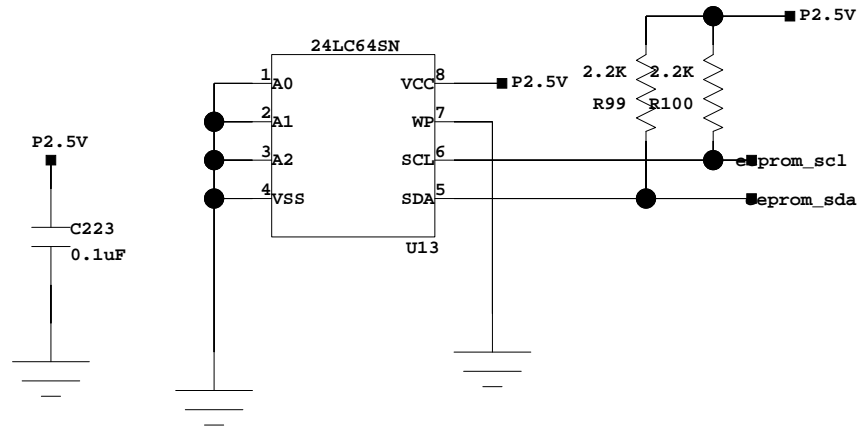


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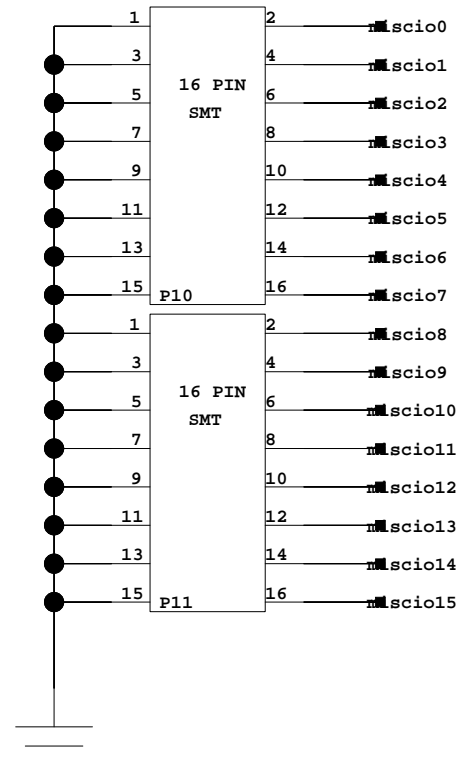
MASTER TIMING CONTROL BOARD
Pizza Box IO _ SFP

Date: 28/06/2016:10:42 DRAWN BY: Jack Fried

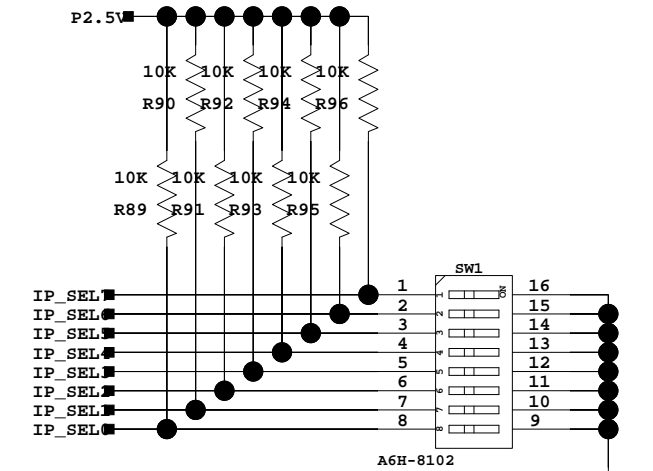
ON BOARD FLASH MEMORY



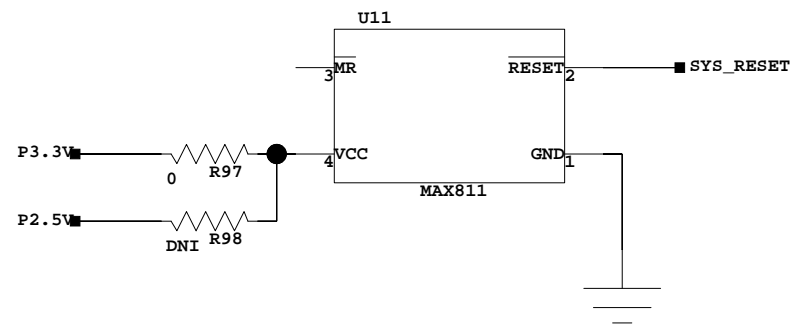
TEST POINTS



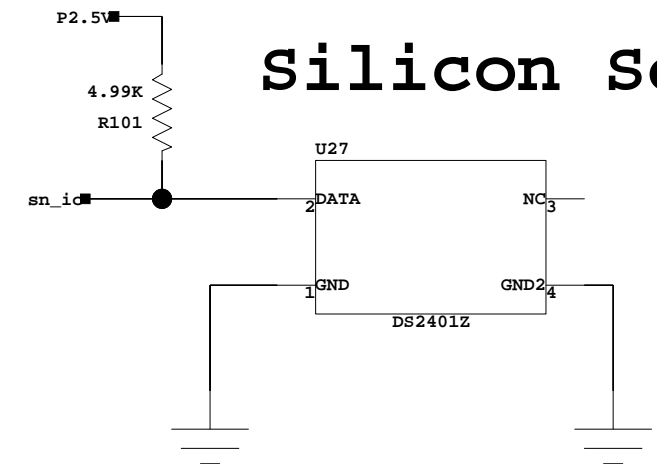
SYSTEM IP SELECTION



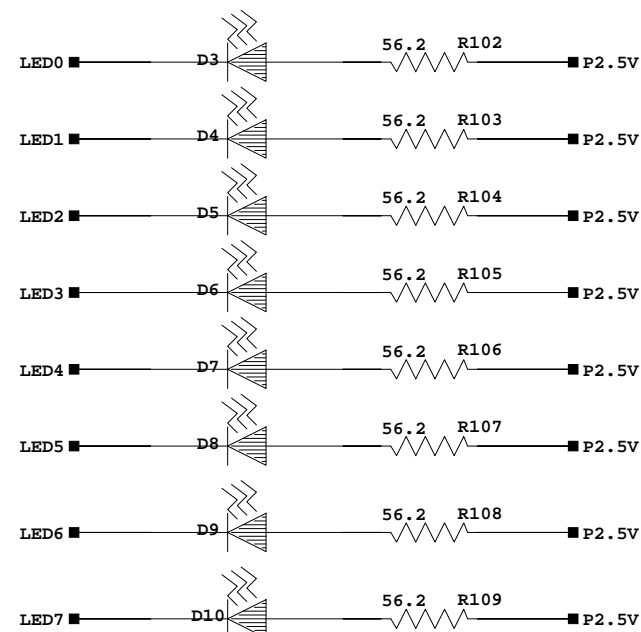
POWER ON RESET



Silicon Serial Number



LEDS



MTC_MISC_IO			
LED0	B22	LED[0]	miscio[15]
LED1	C21	LED[1]	miscio[14]
LED2	D21	LED[2]	miscio[13]
LED3	D22	LED[3]	miscio[12]
LED4	E22	LED[4]	miscio[11]
LED5	E21	LED[5]	miscio[10]
LED6	E20	LED[6]	miscio[9]
LED7	A22	LED[7]	miscio[8]
IP_SEL[0]	A8	IP_SEL[0]	miscio[6]
IP_SEL[1]	A7	IP_SEL[1]	miscio[5]
IP_SEL[2]	B7	IP_SEL[2]	miscio[4]
IP_SEL[3]	B6	IP_SEL[3]	miscio[3]
IP_SEL[4]	B10	IP_SEL[4]	miscio[2]
IP_SEL[5]	C9	IP_SEL[5]	miscio[1]
IP_SEL[6]	C6	IP_SEL[6]	miscio[0]
IP_SEL[7]	C8	IP_SEL[7]	miscio[0]
eeprom_scl	J22	eeprom_scl	SYS_RESET
eeprom_sda	J21	eeprom_sda	sn_io
			AB15 SYS_RESET
			AB13 sn_io

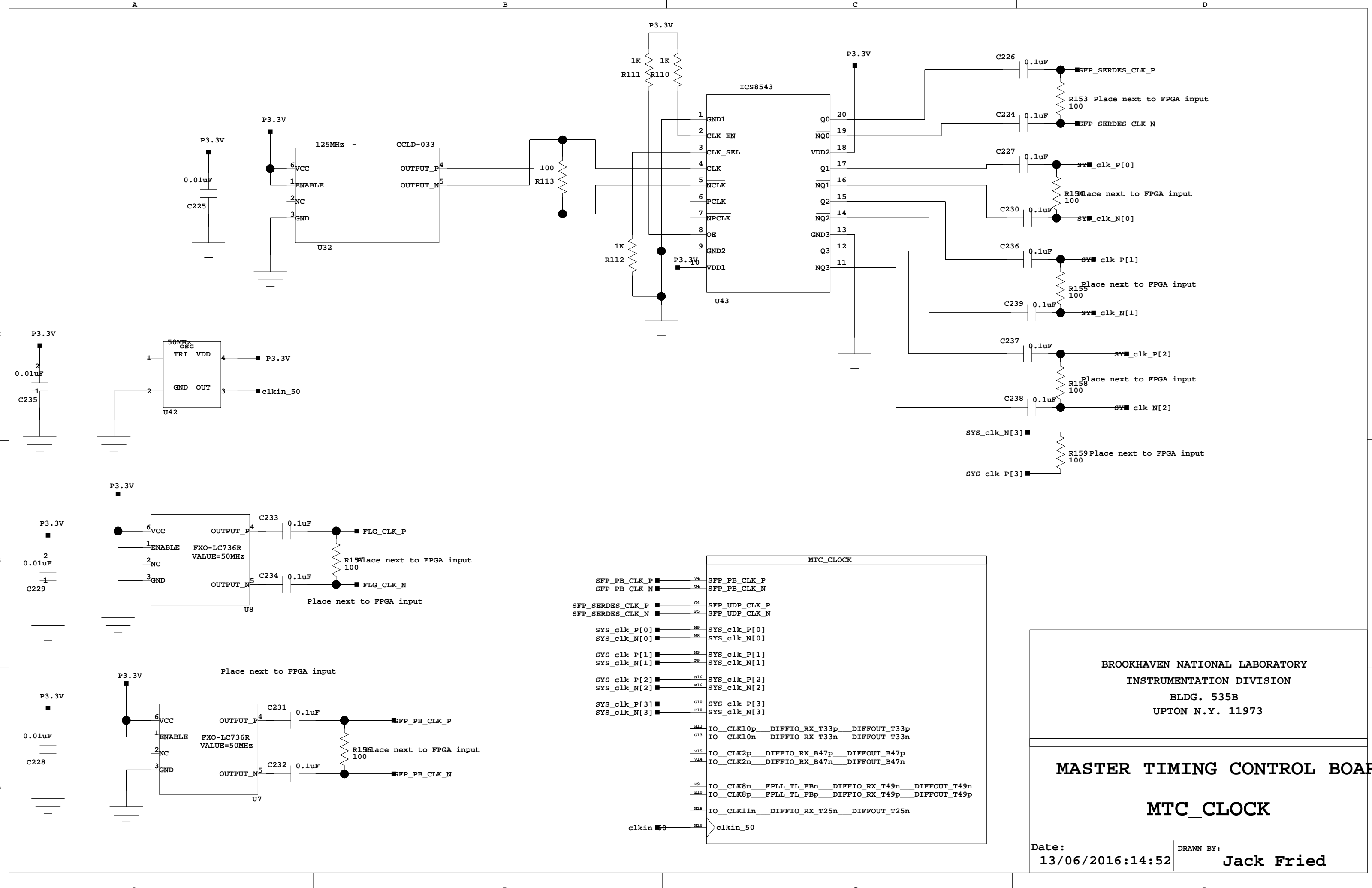
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MASTER TIMING CONTROL BOARD

MTC MISC IO

Date: 02/06/2016:17:21

DRAWN BY: Jack Fried



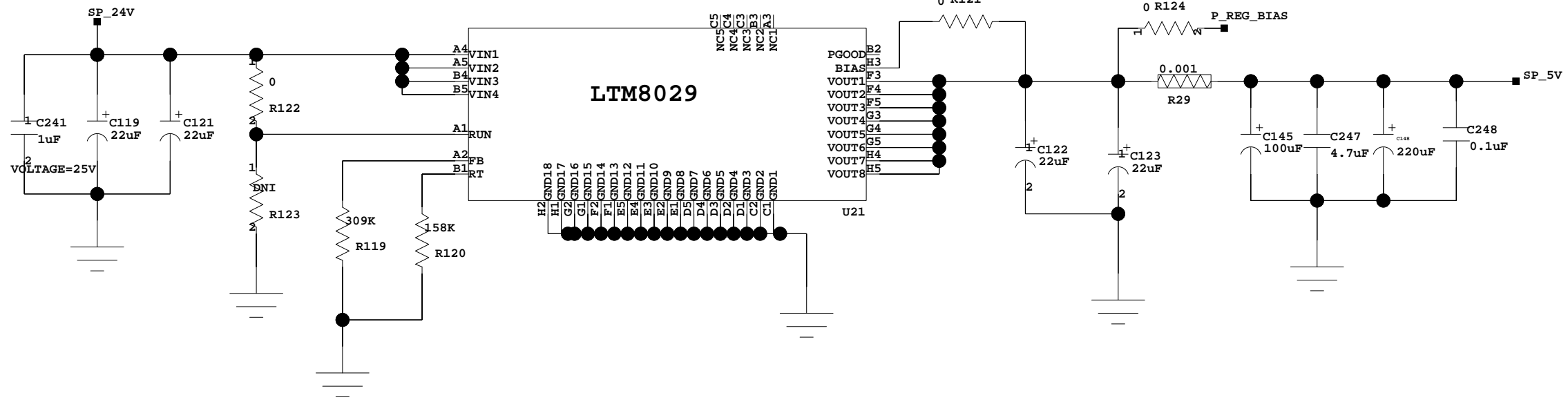
MTC_CLOCK		
SFP_PB_CLK_P	V4	SFP_PB_CLK_P
SFP_PB_CLK_N	U4	SFP_PB_CLK_N
SFP_SERDES_CLK_P	G4	SFP_UDP_CLK_P
SFP_SERDES_CLK_N	F5	SFP_UDP_CLK_N
SYS_clk_P[0]	M9	SYS_clk_P[0]
SYS_clk_N[0]	M8	SYS_clk_N[0]
SYS_clk_P[1]	M9	SYS_clk_P[1]
SYS_clk_N[1]	P9	SYS_clk_N[1]
SYS_clk_P[2]	N16	SYS_clk_P[2]
SYS_clk_N[2]	M16	SYS_clk_N[2]
SYS_clk_P[3]	G10	SYS_clk_P[3]
SYS_clk_N[3]	F10	SYS_clk_N[3]
IO_CLK10p_DIFFIO_RX_T33p_DIFFFOUT_T33p	H13	
IO_CLK10n_DIFFIO_RX_T33n_DIFFFOUT_T33n	G13	
IO_CLK2p_DIFFIO_RX_B47p_DIFFFOUT_B47p	V15	
IO_CLK2n_DIFFIO_RX_B47n_DIFFFOUT_B47n	V14	
IO_CLK8n_FPLL_TL_FBn_DIFFIO_RX_T49n_DIFFFOUT_T49n	F9	
IO_CLK8p_FPLL_TL_FBp_DIFFIO_RX_T49p_DIFFFOUT_T49p	B10	
IO_CLK11n_DIFFIO_RX_T25n_DIFFFOUT_T25n	H15	
clk_in_50	H16	clk_in_50

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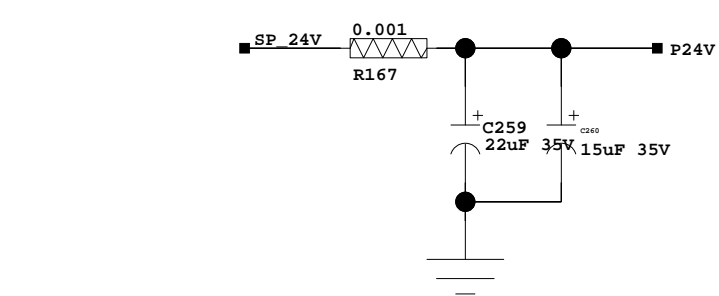
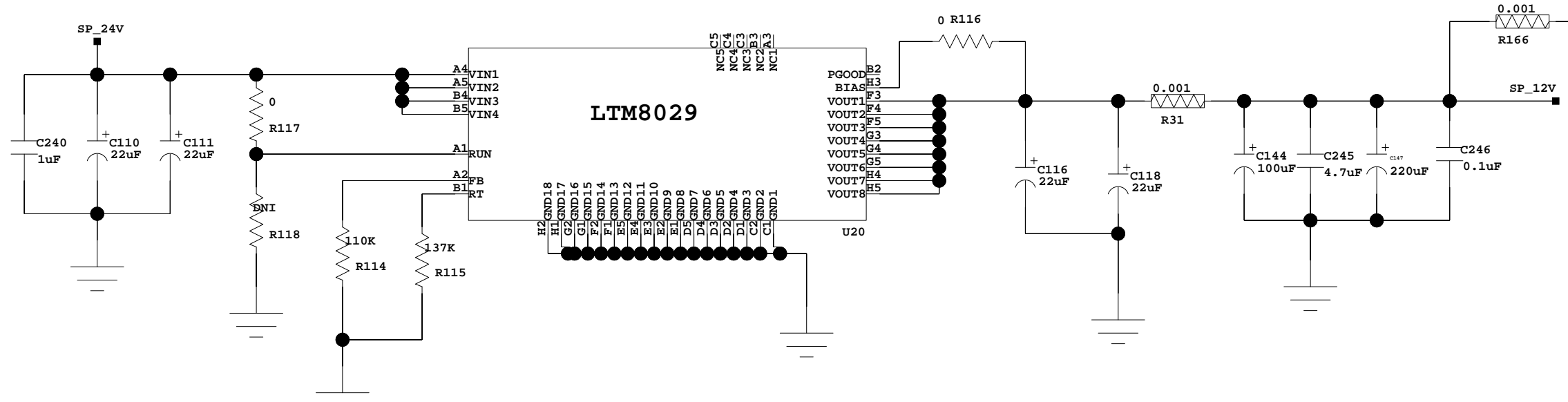
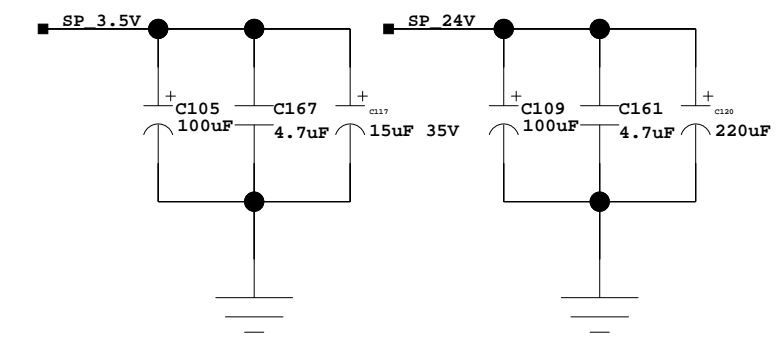
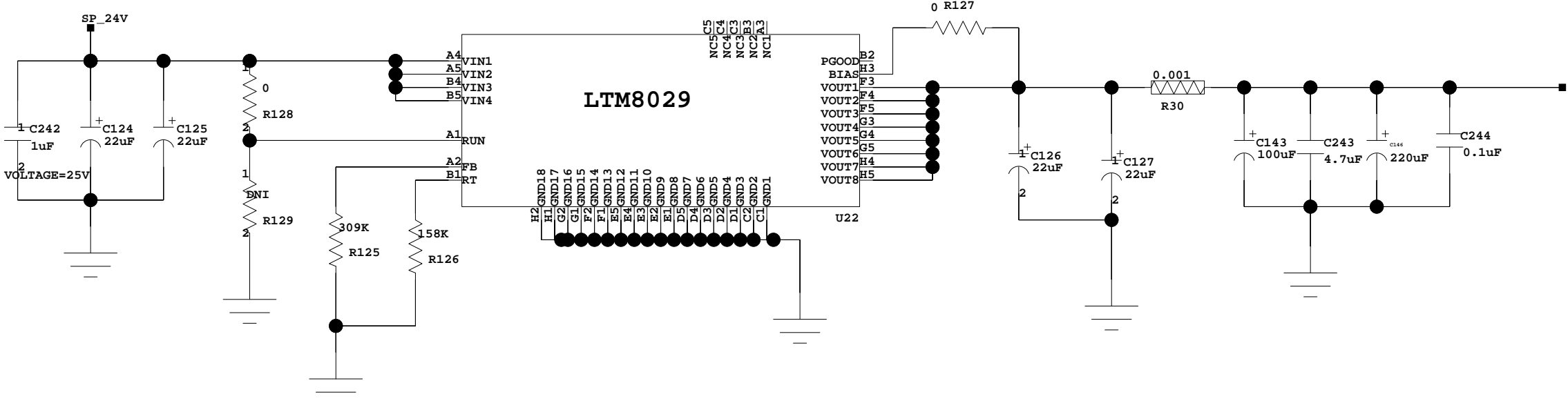
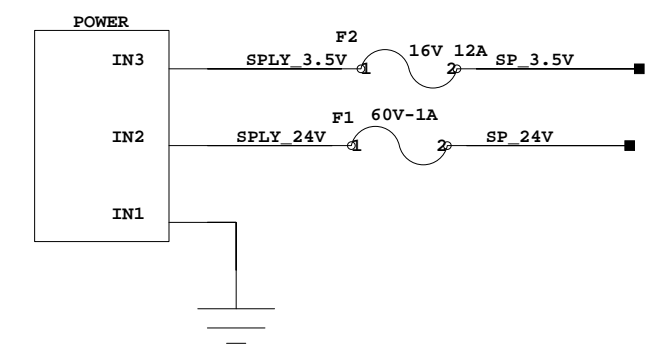
MASTER TIMING CONTROL BOARD

MTC_CLOCK

Date: 13/06/2016:14:52 DRAWN BY: Jack Fried



BOARD POWER INPUT



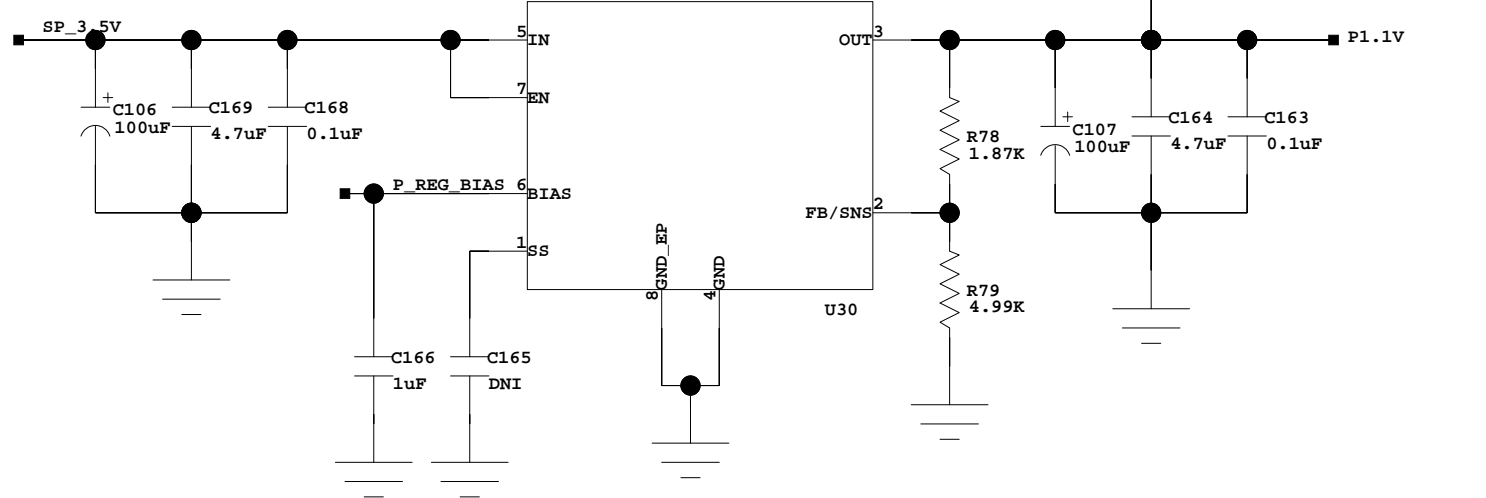
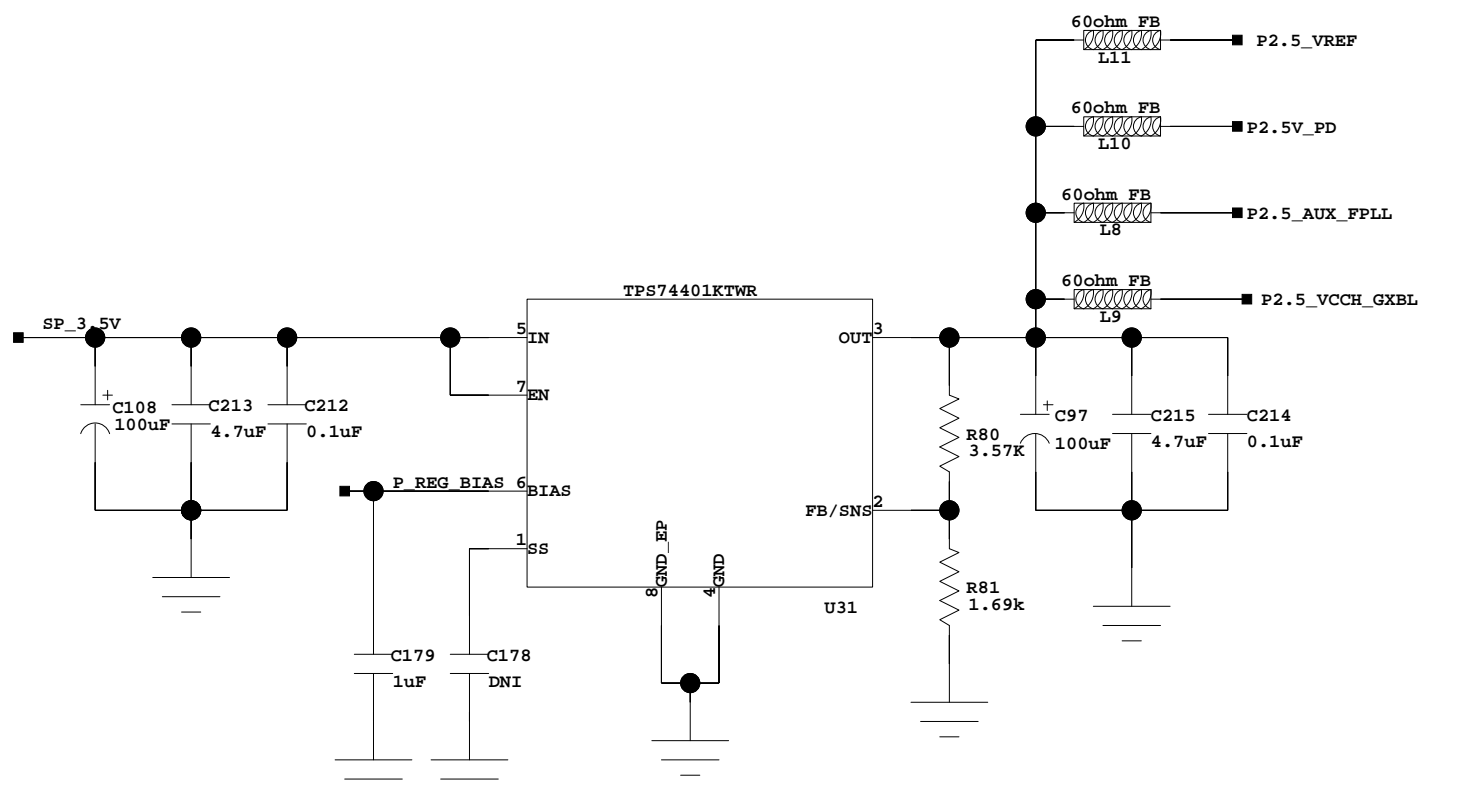
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MASTER TIMING CONTROL BOARD

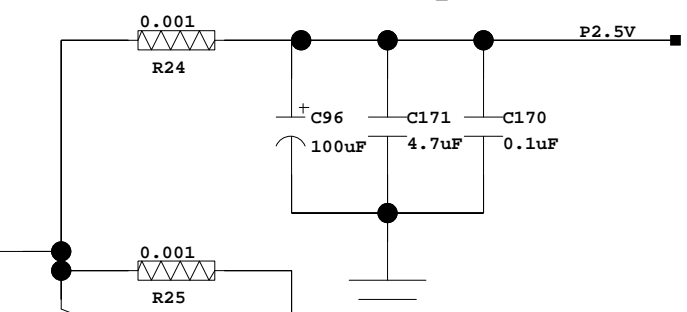
MTC POWER_1

Date: 03/08/2016:11:24	DRAWN BY: Jack Fried
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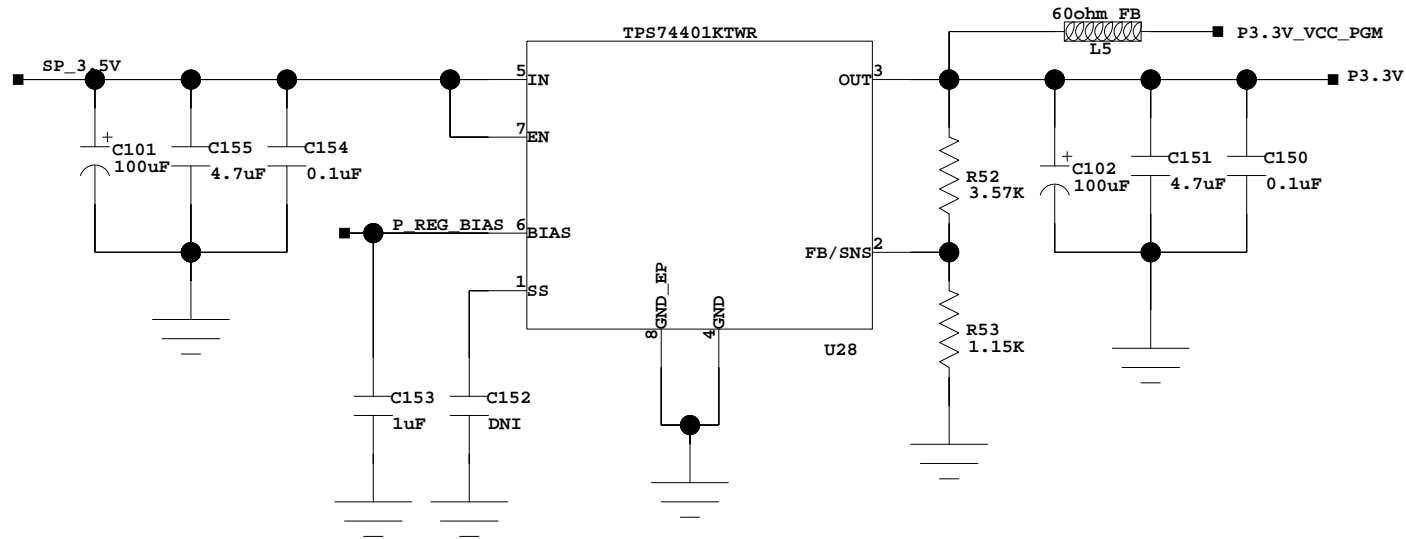
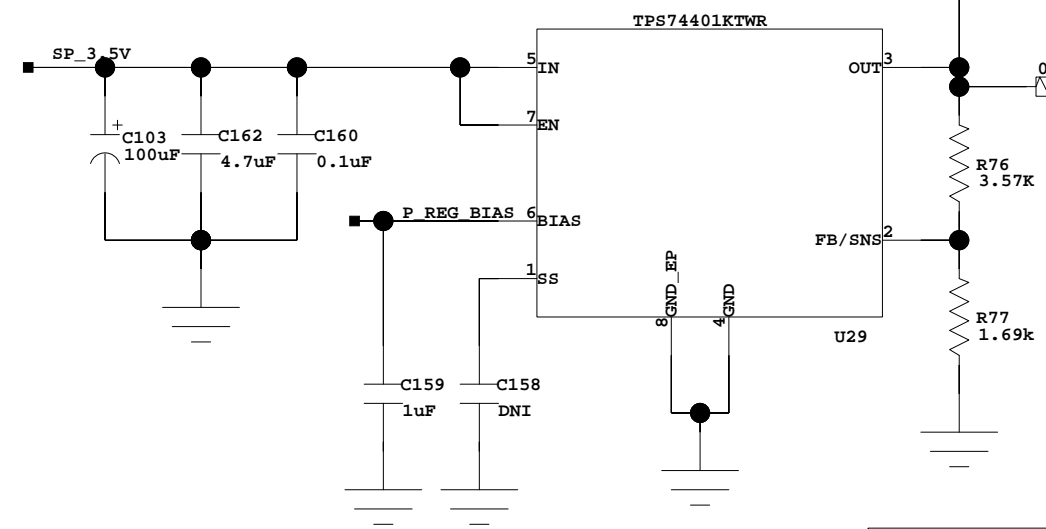
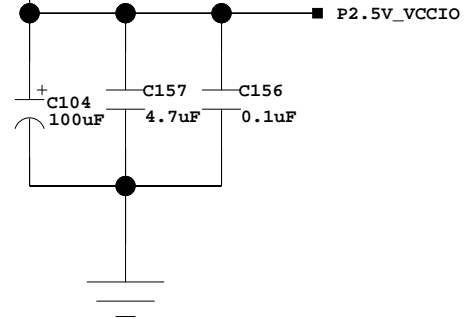
FPGA AUX VOLTAGE 2.5V



Board power 2.5V



FPGA IO BANK VOLTAGE 2.5V



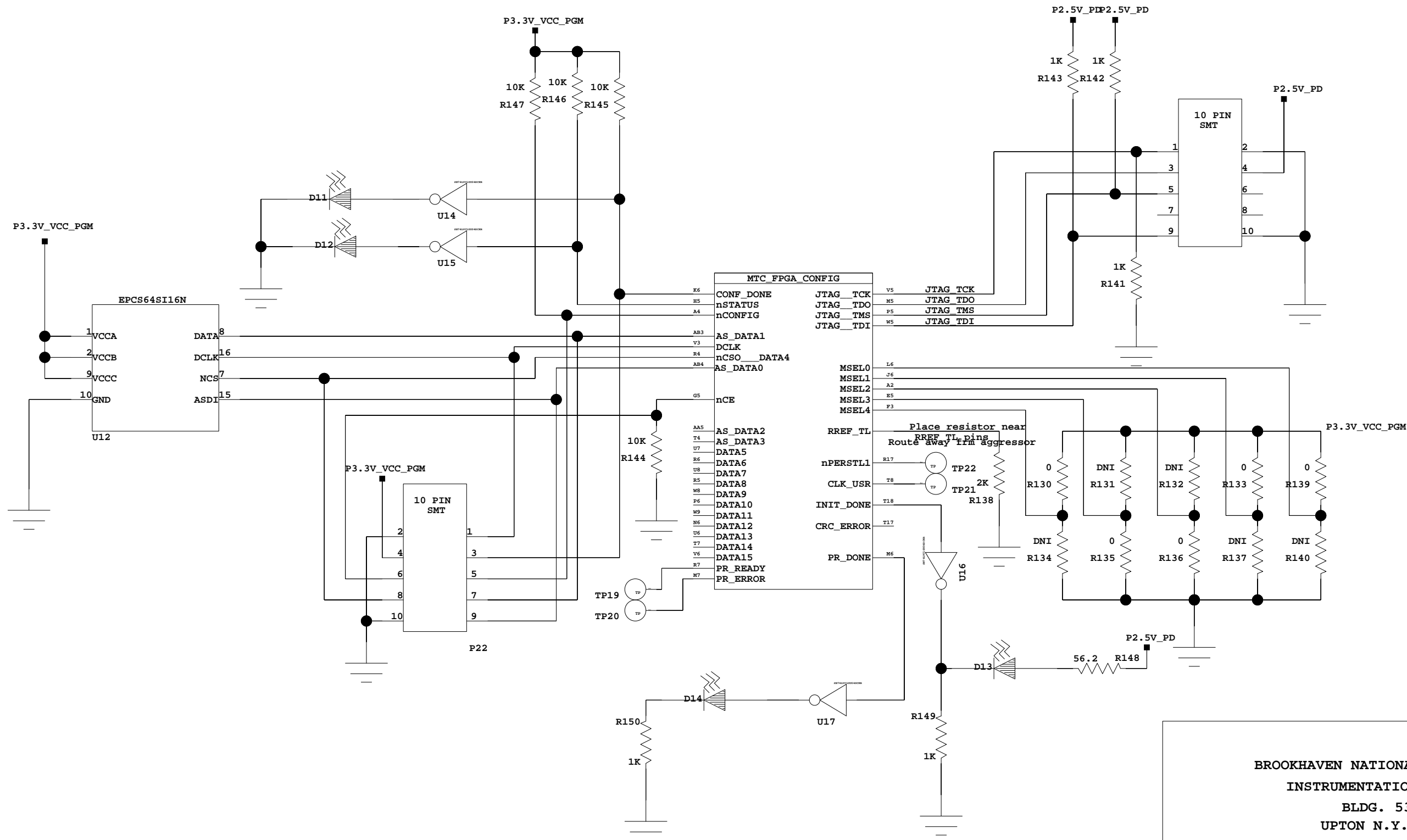
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MASTER TIMING CONTROL BOARD

MTC POWER_2

Date:
 06/07/2016:10:08

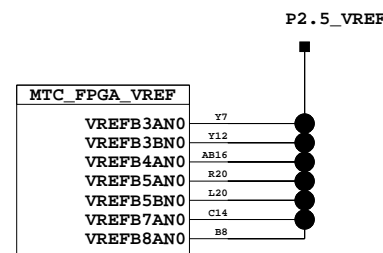
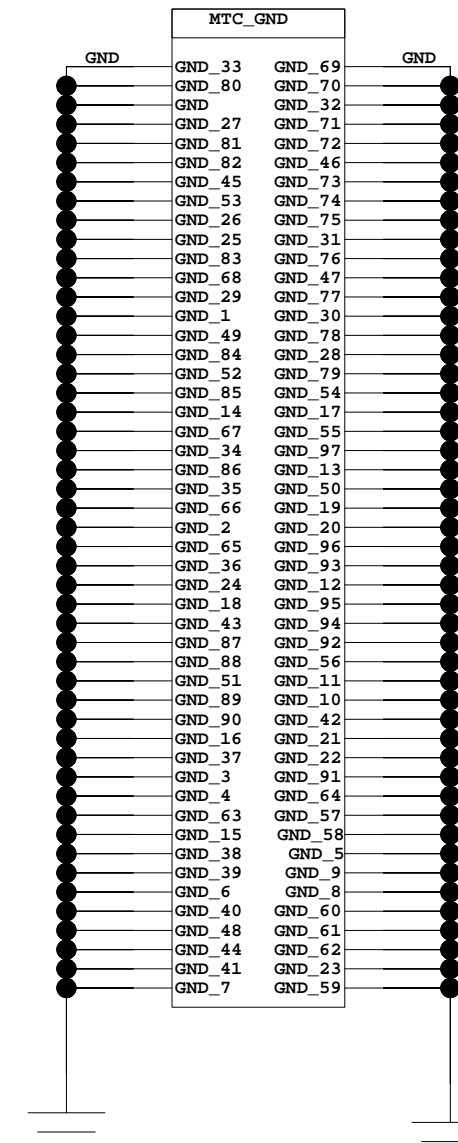
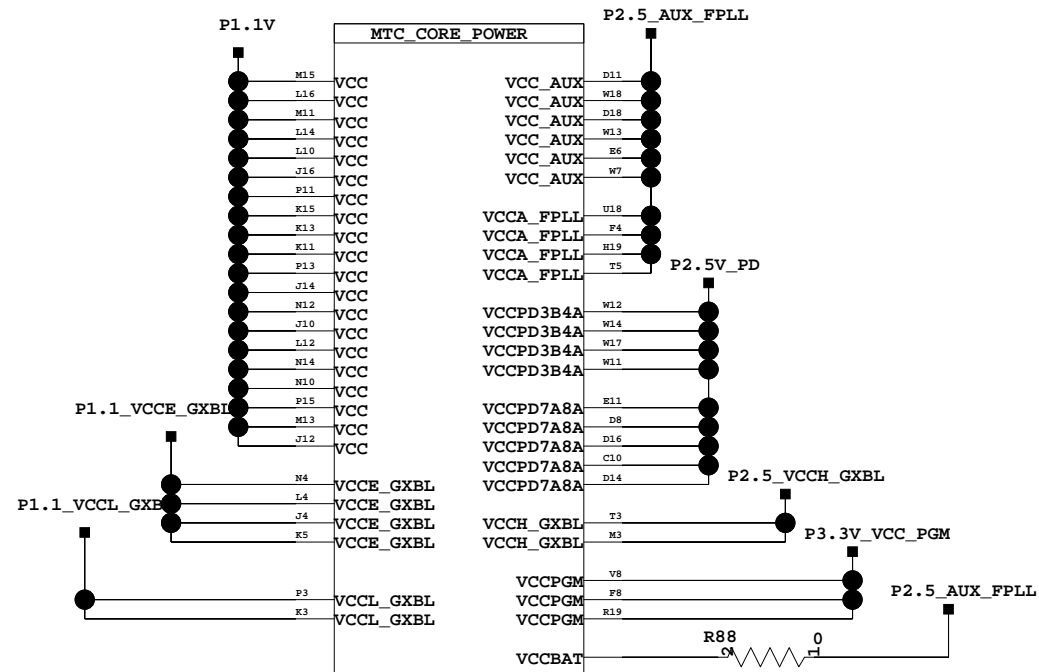
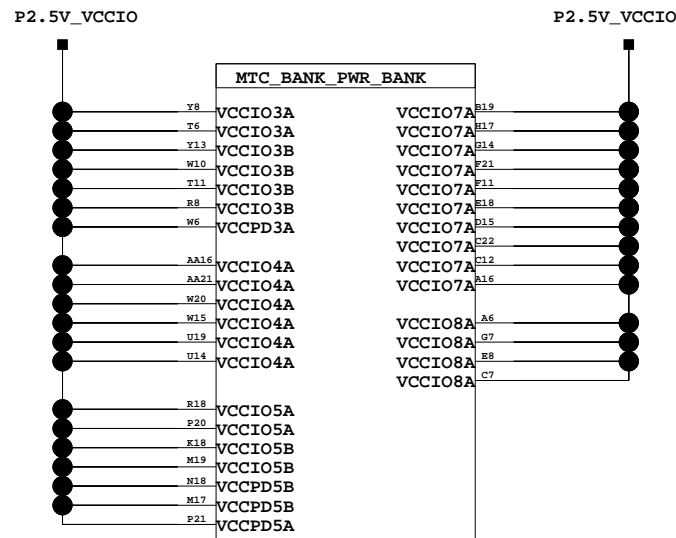
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MASTER TIMING CONTROL BOARD
FPGA CONFIG

Date: 02/06/2016:17:10
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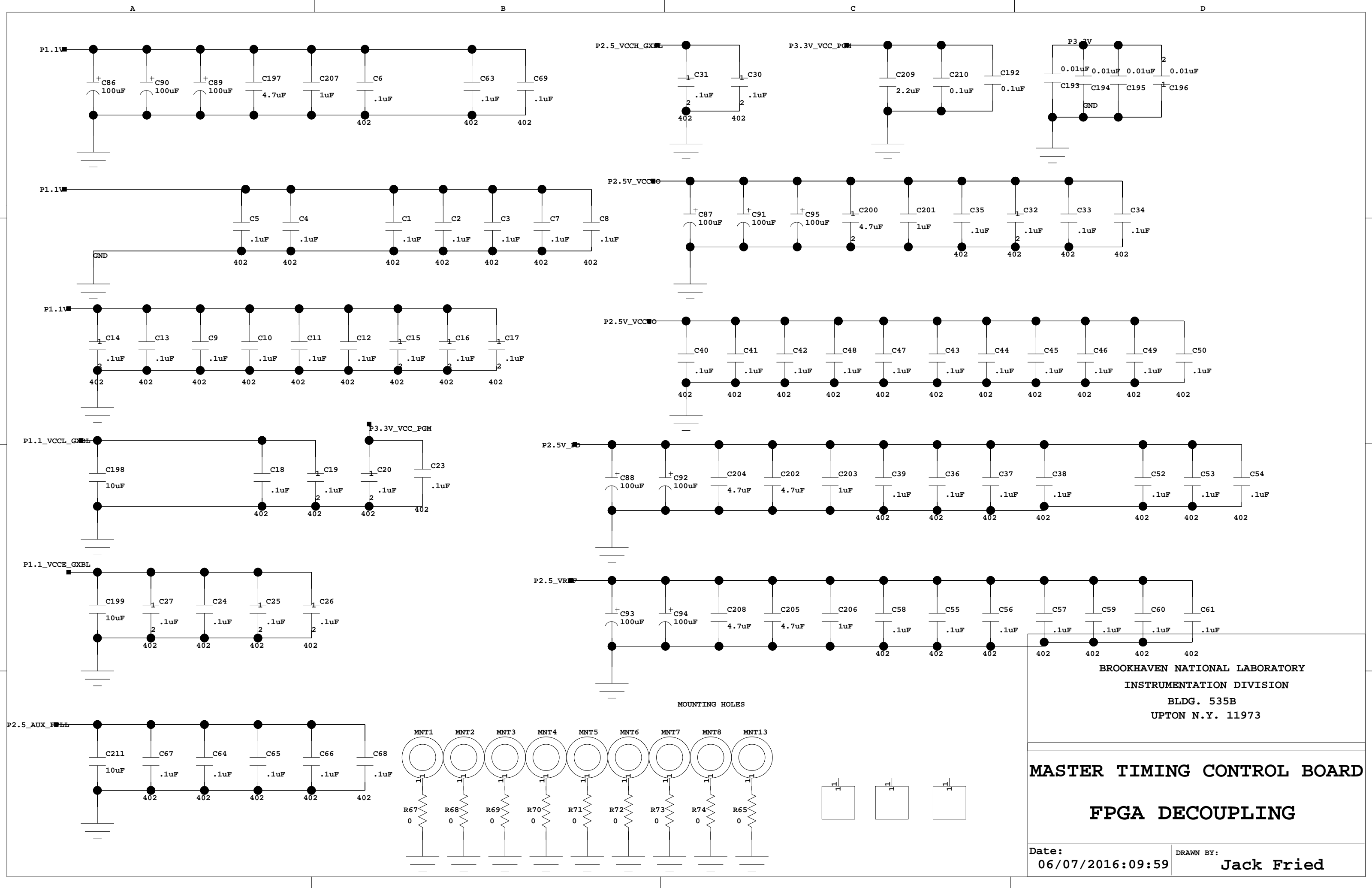


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MASTER TIMING CONTROL BOARD
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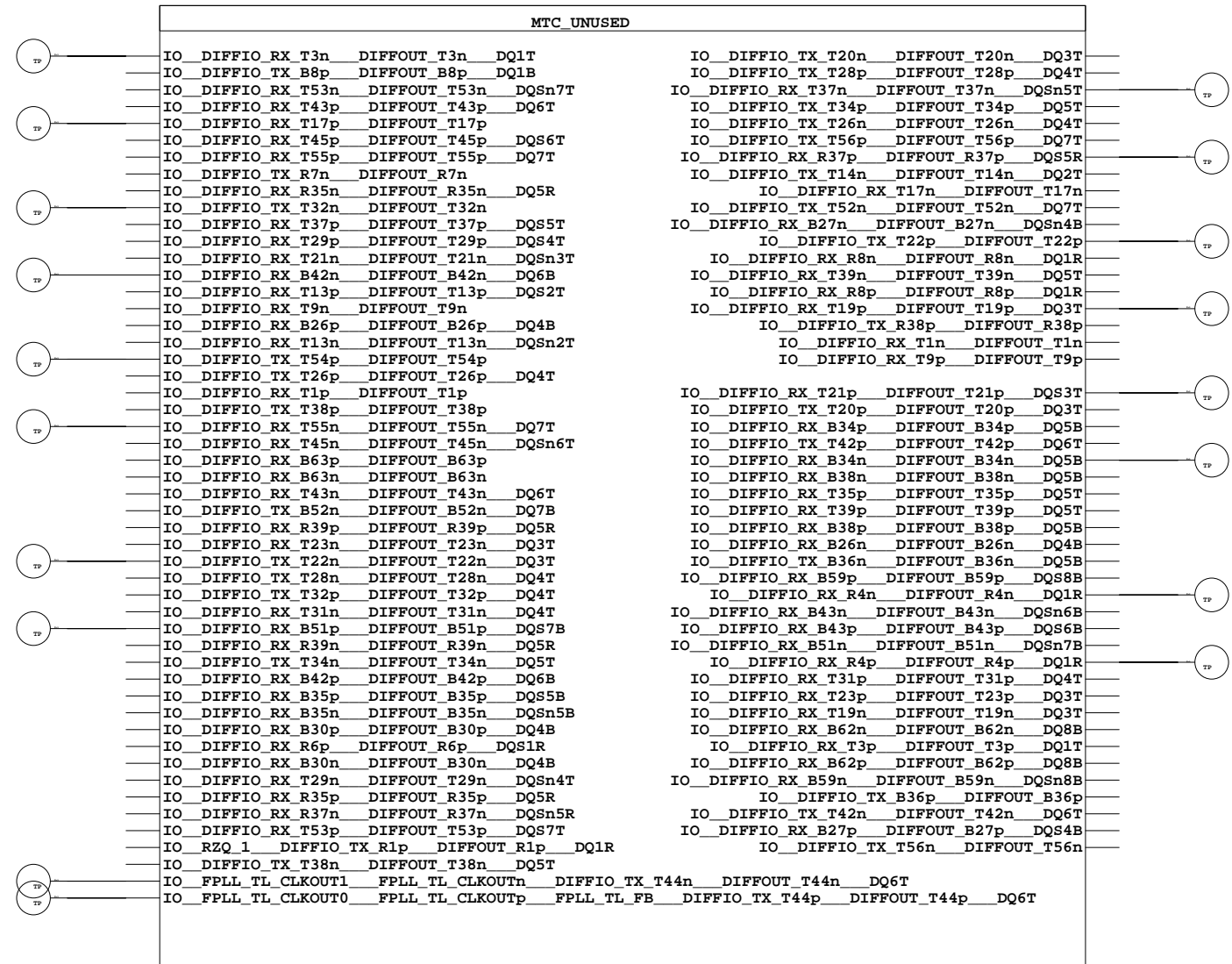
DRAWN BY:
 Jack Fried



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MASTER TIMING CONTROL BOARD
FPGA DECOUPLING

Date: 06/07/2016:09:59
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FPGA UNUSED PINS

Date: 25/05/2016:12:42 DRAWN BY: Jack Fried