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DUNE FM DUAL FPGA

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BROOKHAVEN NATIONAL LABORATORY	
INSTRUMENTATION DIVISION	
<small>TITLE</small>	
TITLE	
<small>SIZE</small>	<small>BOARD : DUNE AM</small>
<small>DRAWN : Jack Fried</small>	<small>DATE : 24/01/2020:17:26</small>

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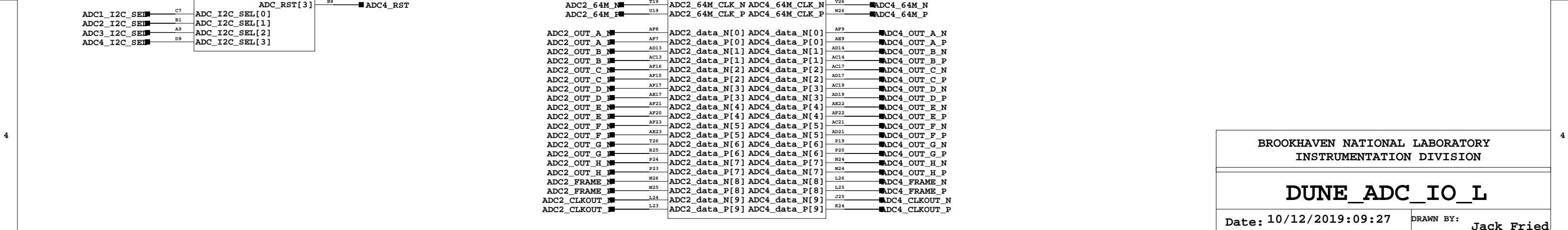
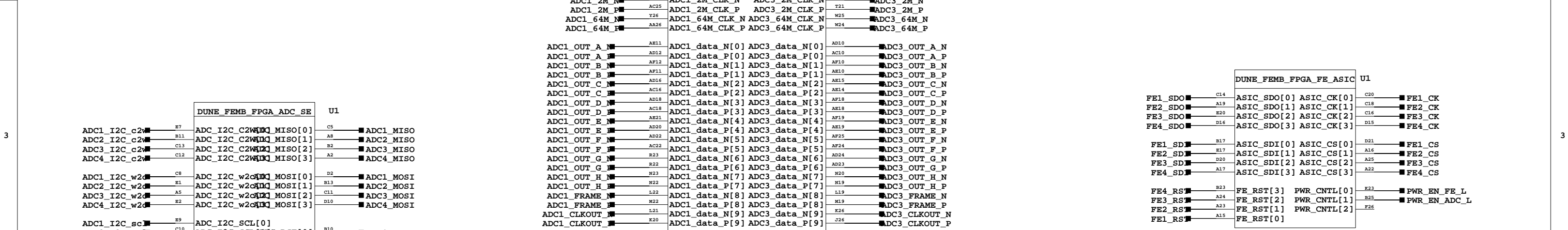
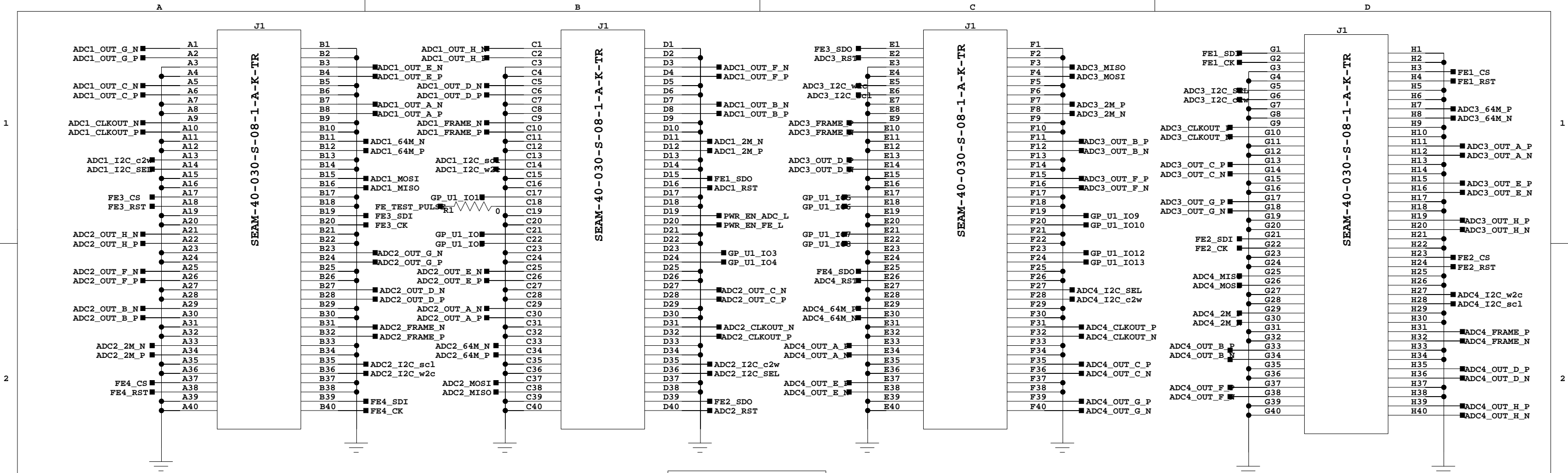
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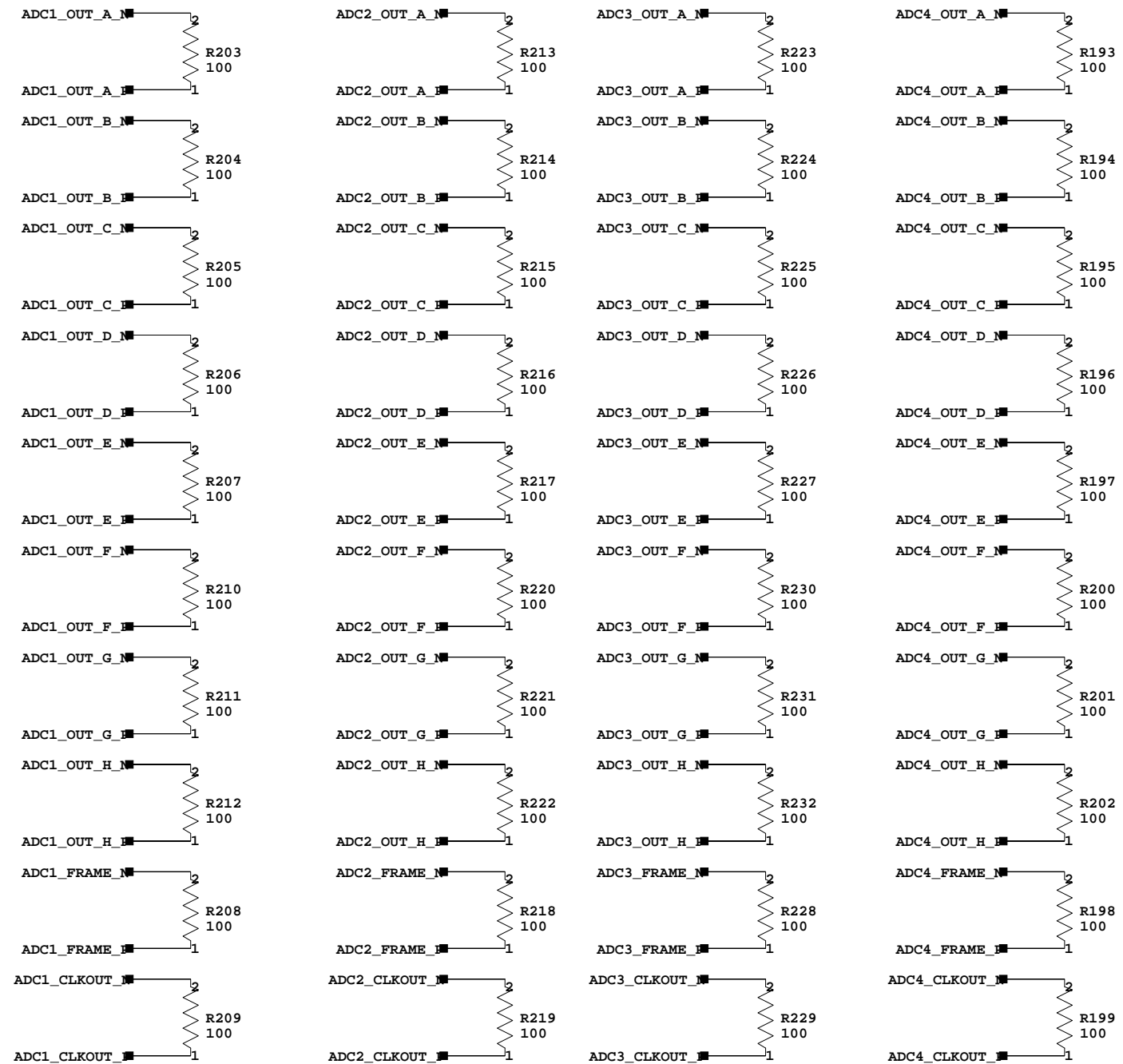
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LVDS TERMINATION PLACE UNDER FPGA



BROOKHAVEN NATIONAL LABORATORY	
INSTRUMENTATION DIVISION	
TITLE	
DUNE FM_TERM L	
SIZE R	BOARD : Schematic1
DRAWN : Jack Fried	DATE : 24/01/2020:17:16

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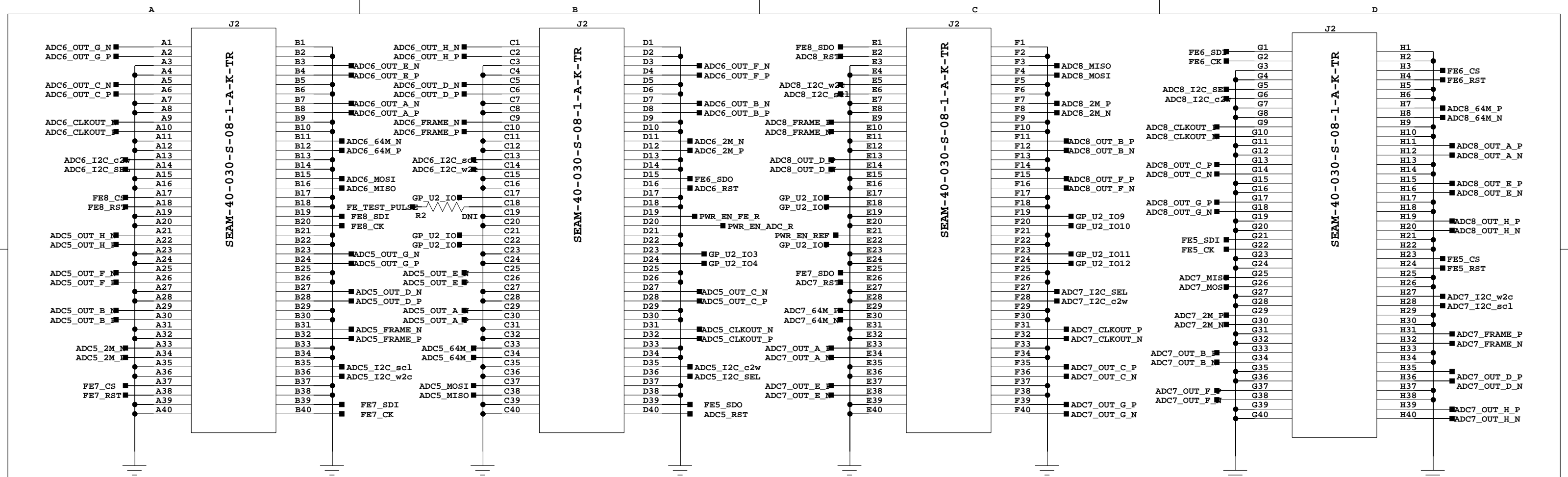
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DUNE_FEMB_FPGA_ADC_SE		U2	
ADC5_I2C_c2w	B7	ADC_I2C_C2W[0] MISO[0]	C5
ADC6_I2C_c2w	B11	ADC_I2C_C2W[1] MISO[1]	A8
ADC7_I2C_c2w	A13	ADC_I2C_C2W[2] MISO[2]	B2
ADC8_I2C_c2w	C12	ADC_I2C_C2W[3] MISO[3]	A2
ADC5_I2C_w2c	C8	ADC_I2C_w2c[0] MOSI[0]	D2
ADC6_I2C_w2c	B1	ADC_I2C_w2c[1] MOSI[1]	B13
ADC7_I2C_w2c	A5	ADC_I2C_w2c[2] MOSI[2]	C11
ADC8_I2C_w2c	B2	ADC_I2C_w2c[3] MOSI[3]	D10
ADC5_I2C_sc	E9	ADC_I2C_SCL[0]	B10
ADC6_I2C_sc	C10	ADC_I2C_SCL[1] ADC_RST[0]	A10
ADC7_I2C_sc	D1	ADC_I2C_SCL[2] ADC_RST[1]	D11
ADC8_I2C_sc	A12	ADC_I2C_SCL[3] ADC_RST[2]	B9
ADC5_I2C_sel	C7	ADC_I2C_SEL[0]	
ADC6_I2C_sel	B1	ADC_I2C_SEL[1]	
ADC7_I2C_sel	A9	ADC_I2C_SEL[2]	
ADC8_I2C_sel	D9	ADC_I2C_SEL[3]	

DUNE_FEMB_FPGA_ADC_DIFFIO			U2		
ADC5_2M_N	AC26	ADC1_2M_CLK_N	ADC3_2M_CLK_N	U22	ADC7_2M_N
ADC5_2M_P	AC25	ADC1_2M_CLK_P	ADC3_2M_CLK_P	T21	ADC7_2M_P
ADC5_64M_N	Y26	ADC1_64M_CLK_N	ADC3_64M_CLK_N	W25	ADC7_64M_N
ADC5_64M_P	AA26	ADC1_64M_CLK_P	ADC3_64M_CLK_P	W24	ADC7_64M_P
ADC5_OUT_A_N	AE11	ADC1_data_N[0]	ADC3_data_N[0]	AD10	ADC7_OUT_A_N
ADC5_OUT_A_P	AD12	ADC1_data_P[0]	ADC3_data_P[0]	AC10	ADC7_OUT_A_P
ADC5_OUT_B_N	AF12	ADC1_data_N[1]	ADC3_data_N[1]	AF10	ADC7_OUT_B_N
ADC5_OUT_B_P	AF11	ADC1_data_P[1]	ADC3_data_P[1]	AE10	ADC7_OUT_B_P
ADC5_OUT_C_N	AD16	ADC1_data_N[2]	ADC3_data_N[2]	AE15	ADC7_OUT_C_N
ADC5_OUT_C_P	AC16	ADC1_data_P[2]	ADC3_data_P[2]	AE14	ADC7_OUT_C_P
ADC5_OUT_D_N	AD18	ADC1_data_N[3]	ADC3_data_N[3]	AF18	ADC7_OUT_D_N
ADC5_OUT_D_P	AC18	ADC1_data_P[3]	ADC3_data_P[3]	AE18	ADC7_OUT_D_P
ADC5_OUT_E_N	AE21	ADC1_data_N[4]	ADC3_data_N[4]	AF19	ADC7_OUT_E_N
ADC5_OUT_E_P	AD20	ADC1_data_P[4]	ADC3_data_P[4]	AE19	ADC7_OUT_E_P
ADC5_OUT_F_N	AD22	ADC1_data_N[5]	ADC3_data_N[5]	AF25	ADC7_OUT_F_N
ADC5_OUT_F_P	AC22	ADC1_data_P[5]	ADC3_data_P[5]	AF24	ADC7_OUT_F_P
ADC5_OUT_G_N	R23	ADC1_data_N[6]	ADC3_data_N[6]	AD24	ADC7_OUT_G_N
ADC5_OUT_G_P	R22	ADC1_data_P[6]	ADC3_data_P[6]	AD23	ADC7_OUT_G_P
ADC5_OUT_H_N	N23	ADC1_data_N[7]	ADC3_data_N[7]	N20	ADC7_OUT_H_N
ADC5_OUT_H_P	N22	ADC1_data_P[7]	ADC3_data_P[7]	N19	ADC7_OUT_H_P
ADC5_FRAME_N	L22	ADC1_data_N[8]	ADC3_data_N[8]	L19	ADC7_FRAME_N
ADC5_FRAME_P	N22	ADC1_data_P[8]	ADC3_data_P[8]	N19	ADC7_FRAME_P
ADC5_CLKOUT_N	L21	ADC1_data_N[9]	ADC3_data_N[9]	K26	ADC7_CLKOUT_N
ADC5_CLKOUT_P	K20	ADC1_data_P[9]	ADC3_data_P[9]	J26	ADC7_CLKOUT_P
ADC6_2M_N	AB26	ADC2_2M_CLK_N	ADC4_2M_CLK_N	Y25	ADC8_2M_N
ADC6_2M_P	AA25	ADC2_2M_CLK_P	ADC4_2M_CLK_P	T24	ADC8_2M_P
ADC6_64M_N	T19	ADC2_64M_CLK_N	ADC4_64M_CLK_N	Y26	ADC8_64M_N
ADC6_64M_P	U19	ADC2_64M_CLK_P	ADC4_64M_CLK_P	W26	ADC8_64M_P
ADC6_OUT_A_N	AF8	ADC2_data_N[0]	ADC4_data_N[0]	AF9	ADC8_OUT_A_N
ADC6_OUT_A_P	AD13	ADC2_data_P[0]	ADC4_data_P[0]	AE9	ADC8_OUT_A_P
ADC6_OUT_B_N	AC13	ADC2_data_N[1]	ADC4_data_N[1]	AD14	ADC8_OUT_B_N
ADC6_OUT_B_P	AF16	ADC2_data_P[1]	ADC4_data_P[1]	AC14	ADC8_OUT_B_P
ADC6_OUT_C_N	AF15	ADC2_data_N[2]	ADC4_data_N[2]	AC17	ADC8_OUT_C_N
ADC6_OUT_C_P	AF17	ADC2_data_P[2]	ADC4_data_P[2]	AD17	ADC8_OUT_C_P
ADC6_OUT_D_N	AE17	ADC2_data_N[3]	ADC4_data_N[3]	AC19	ADC8_OUT_D_N
ADC6_OUT_D_P	AE17	ADC2_data_P[3]	ADC4_data_P[3]	AD19	ADC8_OUT_D_P
ADC6_OUT_E_N	AF20	ADC2_data_N[4]	ADC4_data_N[4]	AE22	ADC8_OUT_E_N
ADC6_OUT_E_P	AF23	ADC2_data_P[4]	ADC4_data_P[4]	AF22	ADC8_OUT_E_P
ADC6_OUT_F_N	AE23	ADC2_data_N[5]	ADC4_data_N[5]	AC21	ADC8_OUT_F_N
ADC6_OUT_F_P	AE23	ADC2_data_P[5]	ADC4_data_P[5]	AD21	ADC8_OUT_F_P
ADC6_OUT_G_N	T26	ADC2_data_N[6]	ADC4_data_P[6]	P19	ADC8_OUT_G_N
ADC6_OUT_G_P	P24	ADC2_data_P[6]	ADC4_data_N[6]	P20	ADC8_OUT_G_P
ADC6_OUT_H_N	P23	ADC2_data_N[7]	ADC4_data_P[7]	N24	ADC8_OUT_H_N
ADC6_OUT_H_P	N26	ADC2_data_P[7]	ADC4_data_N[7]	N24	ADC8_OUT_H_P
ADC6_FRAME_N	N25	ADC2_data_N[8]	ADC4_data_N[8]	L26	ADC8_FRAME_N
ADC6_FRAME_P	L24	ADC2_data_P[8]	ADC4_data_P[8]	L25	ADC8_FRAME_P
ADC6_CLKOUT_N	L24	ADC2_data_N[9]	ADC4_data_N[9]	J25	ADC8_CLKOUT_N
ADC6_CLKOUT_P	L23	ADC2_data_P[9]	ADC4_data_P[9]	K24	ADC8_CLKOUT_P

DUNE_FEMB_FPGA_FE_ASIC			U2		
FE5_SDO	C14	ASIC_SDO[0]	ASIC_CK[0]	C20	FE5_CK
FE6_SDO	A19	ASIC_SDO[1]	ASIC_CK[1]	C18	FE6_CK
FE7_SDO	R20	ASIC_SDO[2]	ASIC_CK[2]	C16	FE7_CK
FE8_SDO	D16	ASIC_SDO[3]	ASIC_CK[3]	D15	FE8_CK
FE5_SDI	B17	ASIC_SDI[0]	ASIC_CS[0]	D21	FE5_CS
FE6_SDI	E17	ASIC_SDI[1]	ASIC_CS[1]	A16	FE6_CS
FE7_SDI	D20	ASIC_SDI[2]	ASIC_CS[2]	A25	FE7_CS
FE8_SDI	A17	ASIC_SDI[3]	ASIC_CS[3]	A22	FE8_CS
FE_RST[3]	R23	FE_RST[3]	PWR_CNTL[0]	K23	PWR_EN_FE_R
FE7_RST[2]	A24	FE_RST[2]	PWR_CNTL[1]	B25	PWR_EN_ADC_R
FE6_RST[1]	A23	FE_RST[1]	PWR_CNTL[2]	F26	PWR_EN_REF
FE5_RST[0]	A15	FE_RST[0]			

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DUNE_ADC_IO_R

Date: 24/01/2020:17:16 DRAWN BY: Jack Fried

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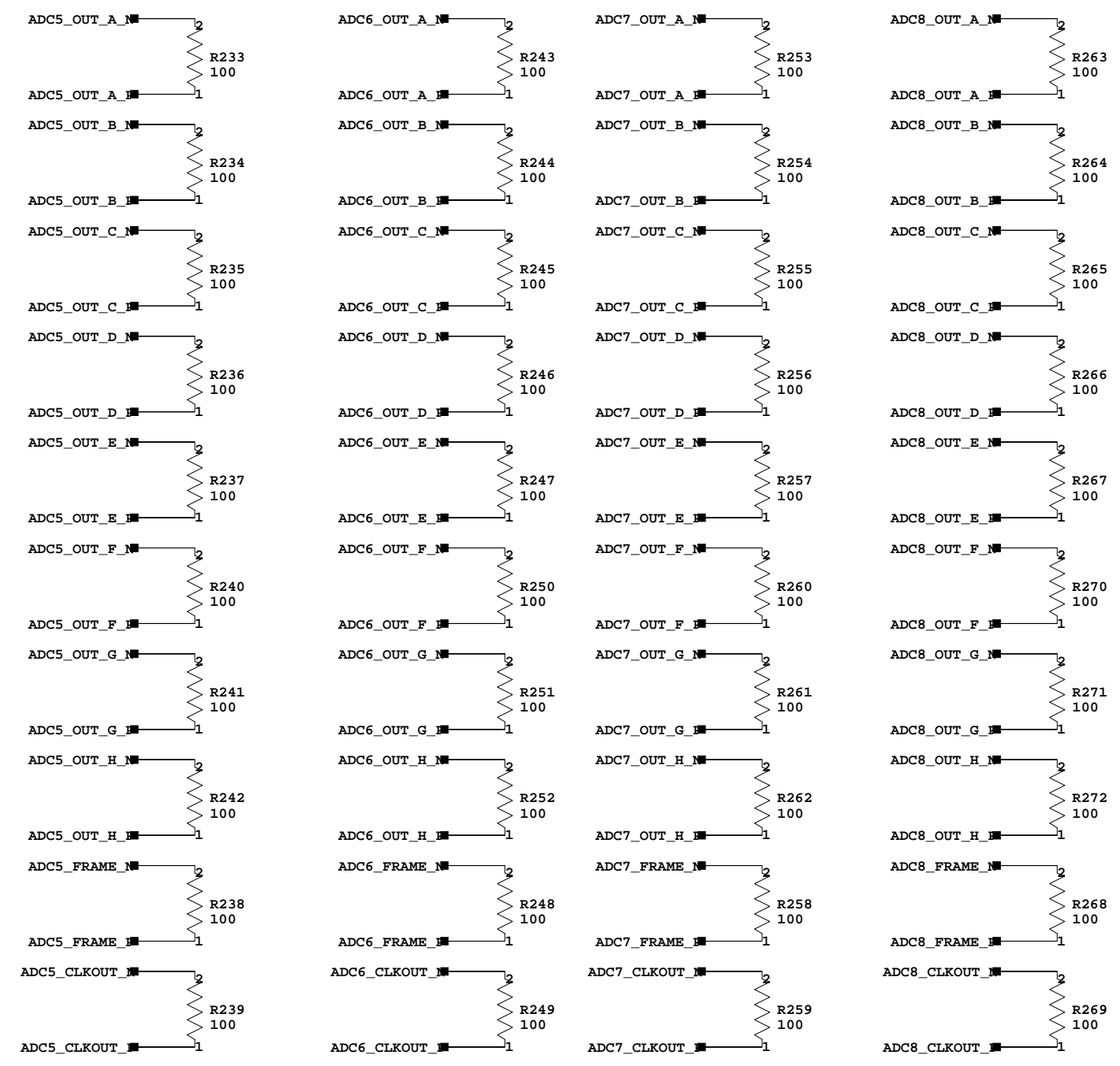
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LVDS TERMINATION

PLACE UNDER FPGA



BROOKHAVEN NATIONAL LABORATORY	
INSTRUMENTATION DIVISION	
TITLE	
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SIZE R	BOARD : Schematic1
DRAWN : Jack Fried	DATE : 24/01/2020:17:16

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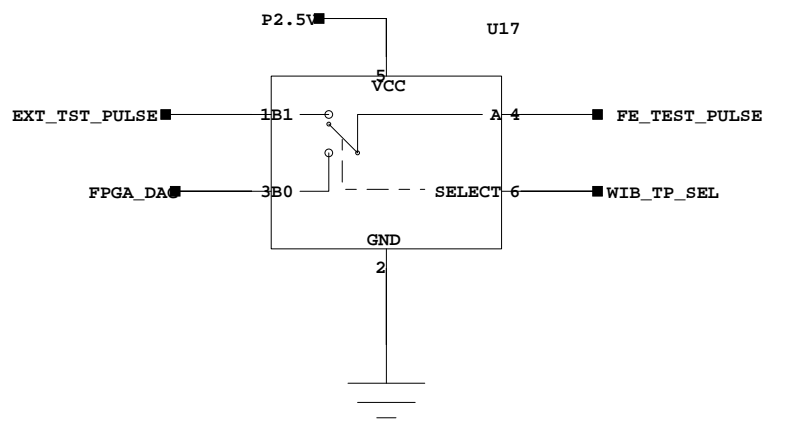
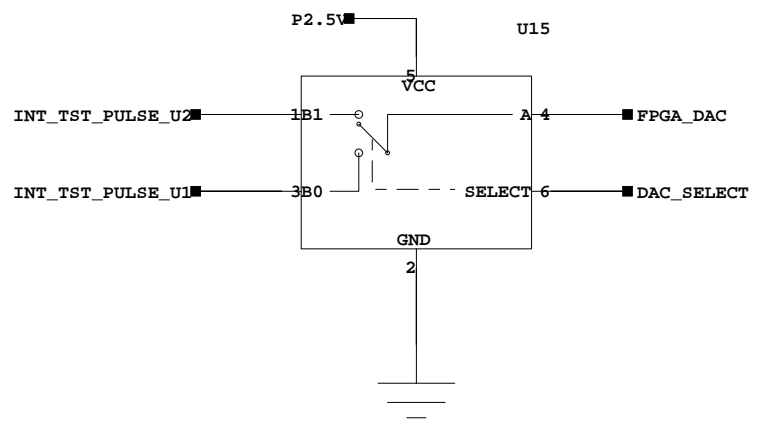
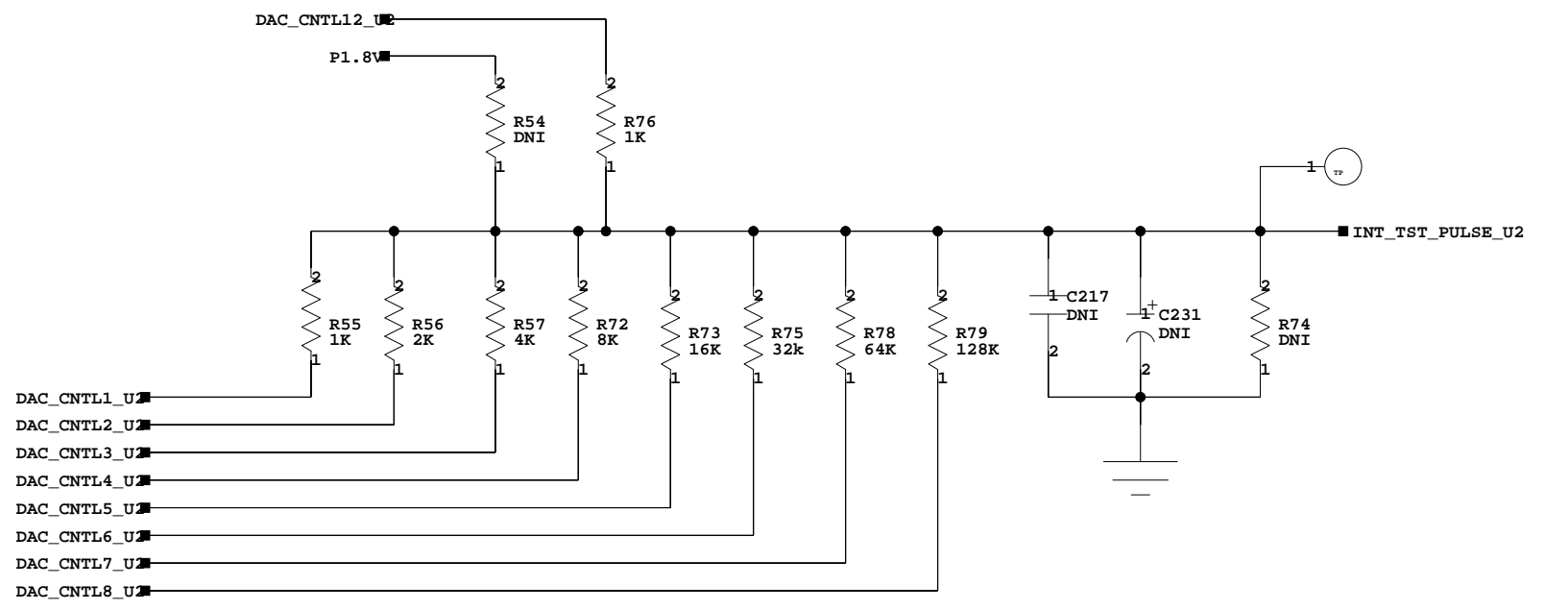
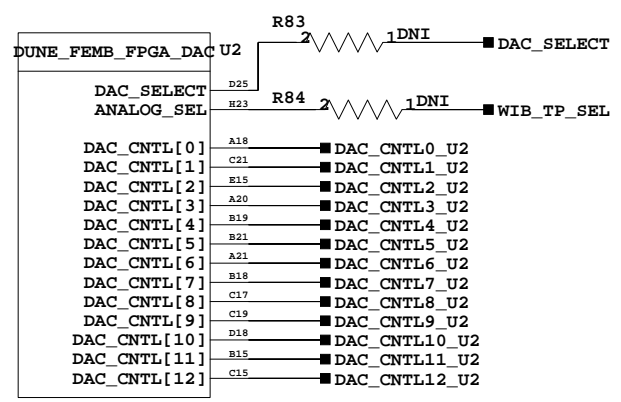
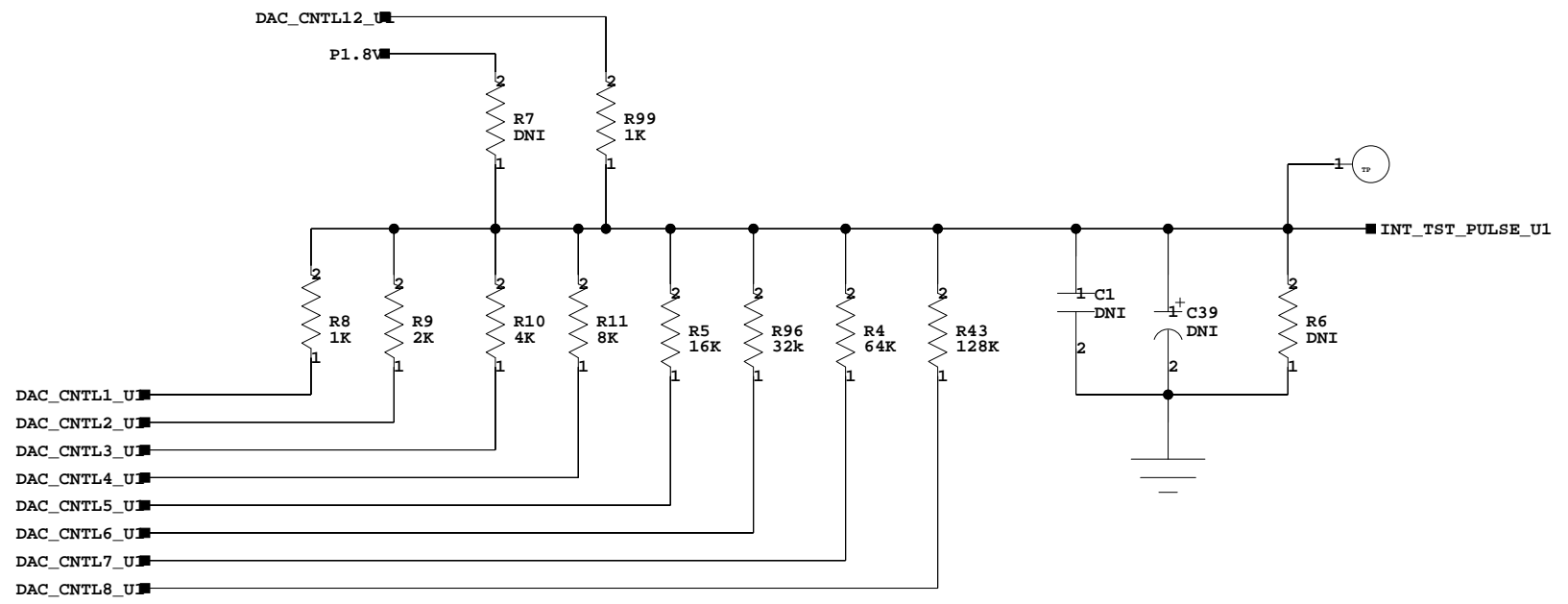
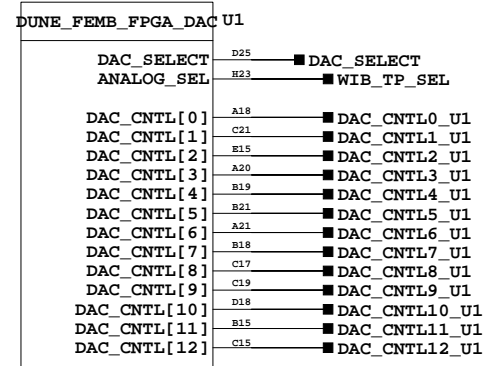
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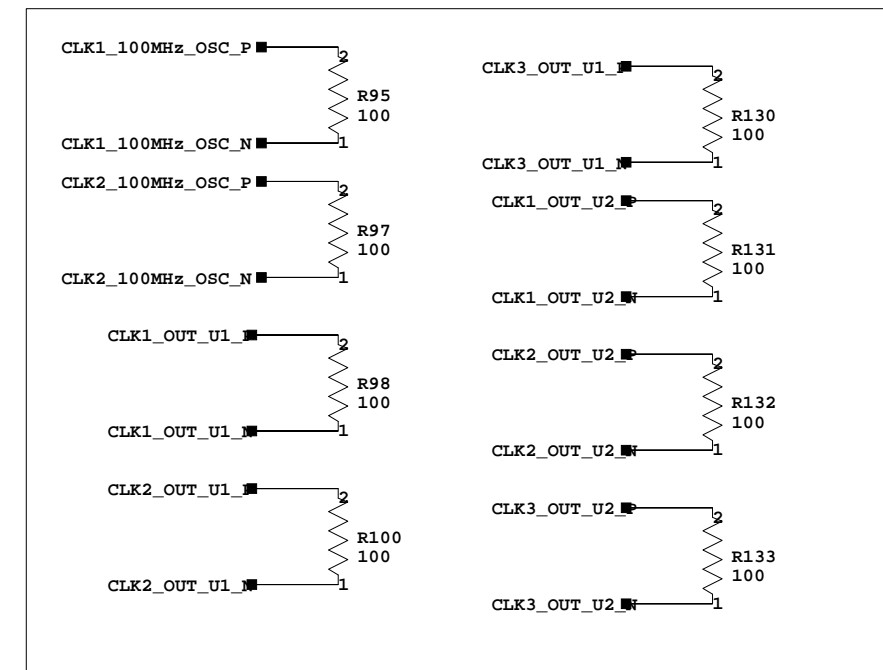
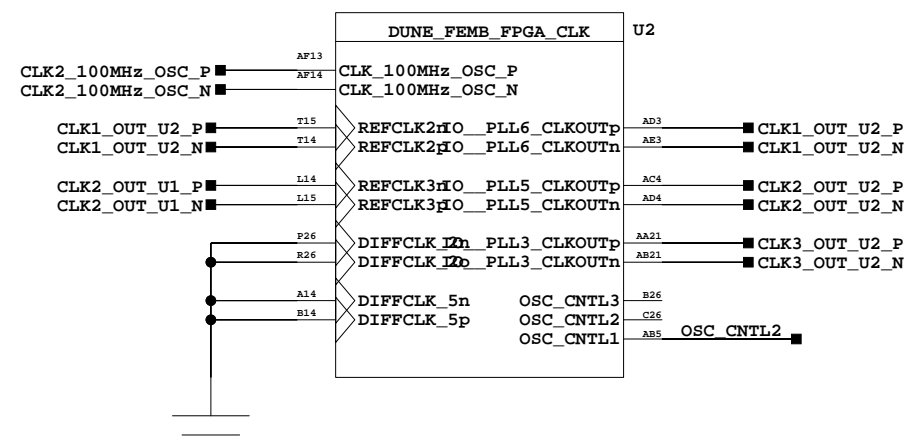
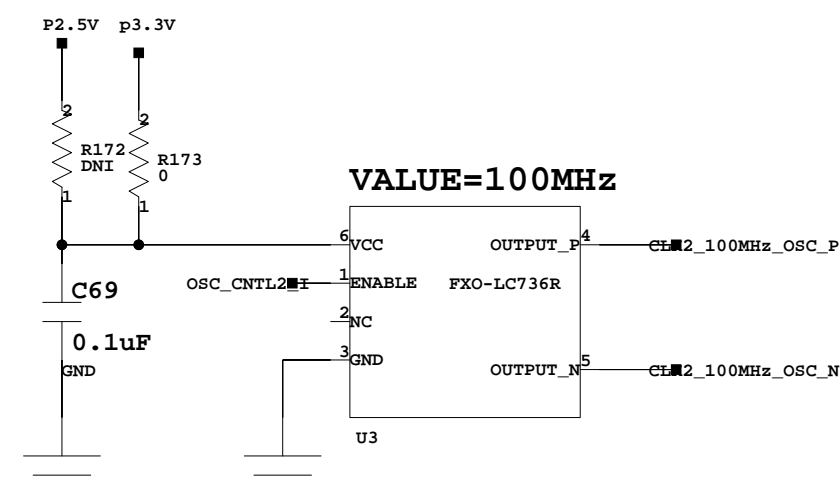
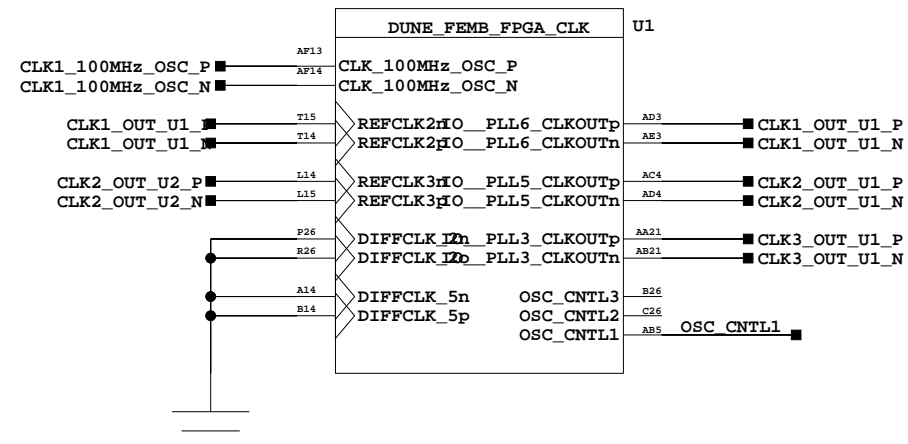
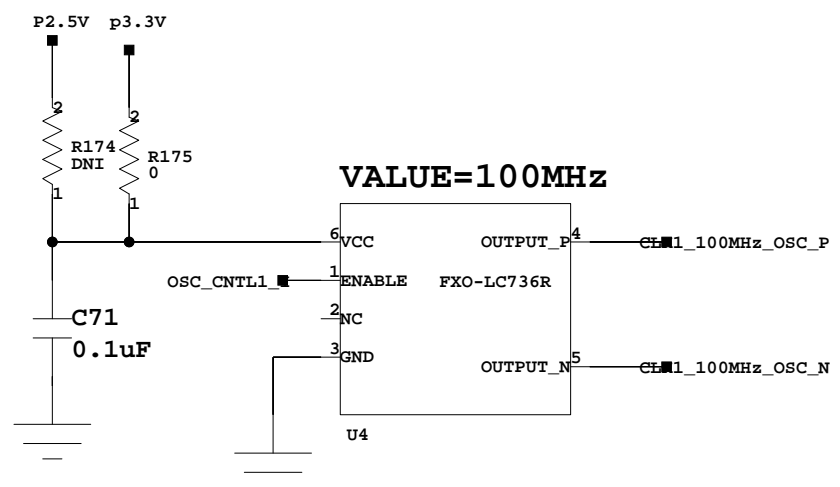
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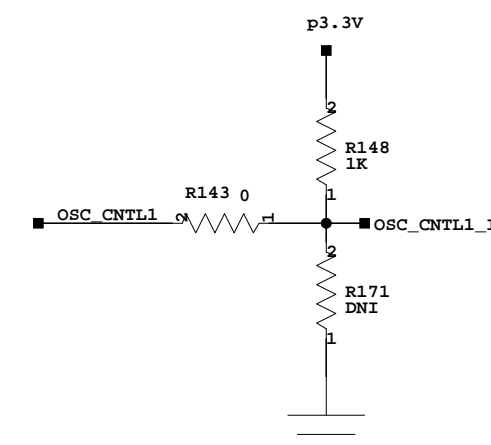
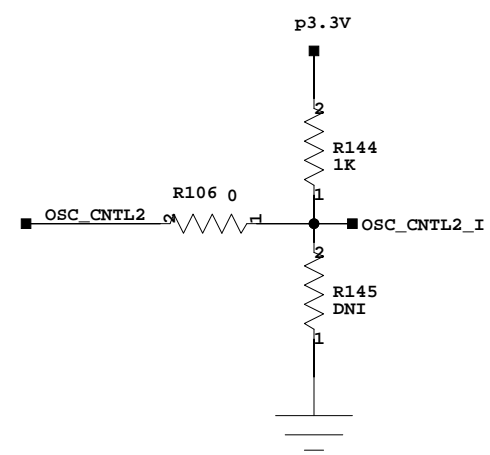
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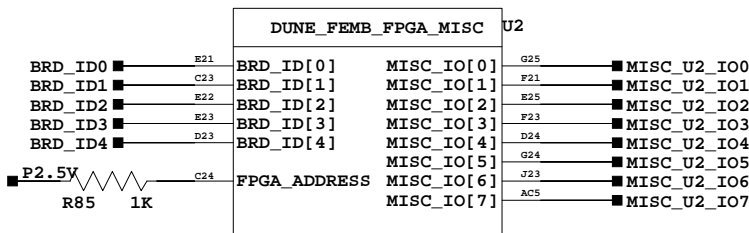
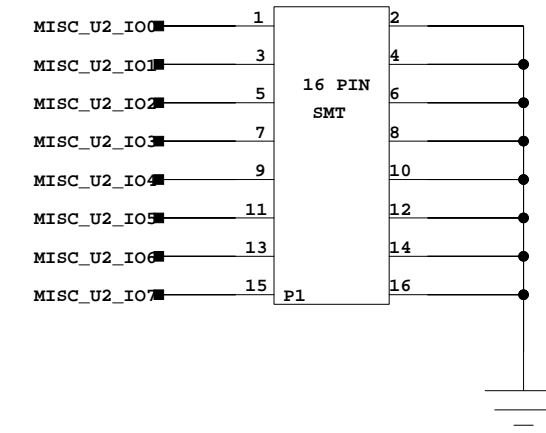
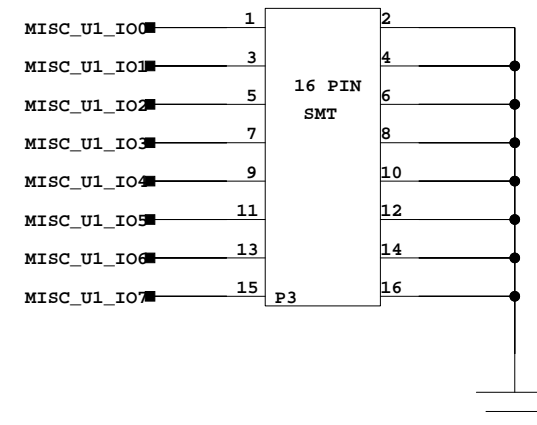
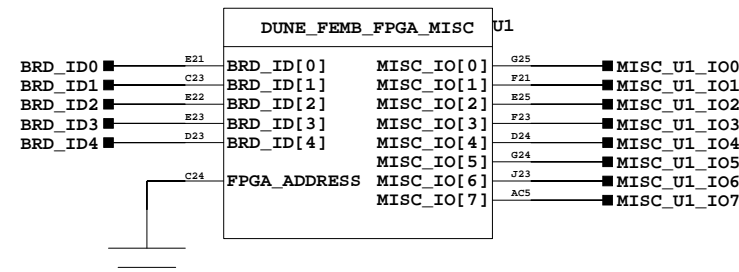
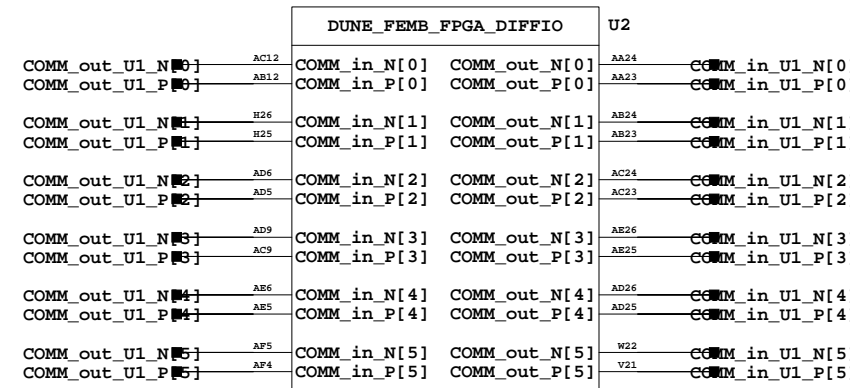
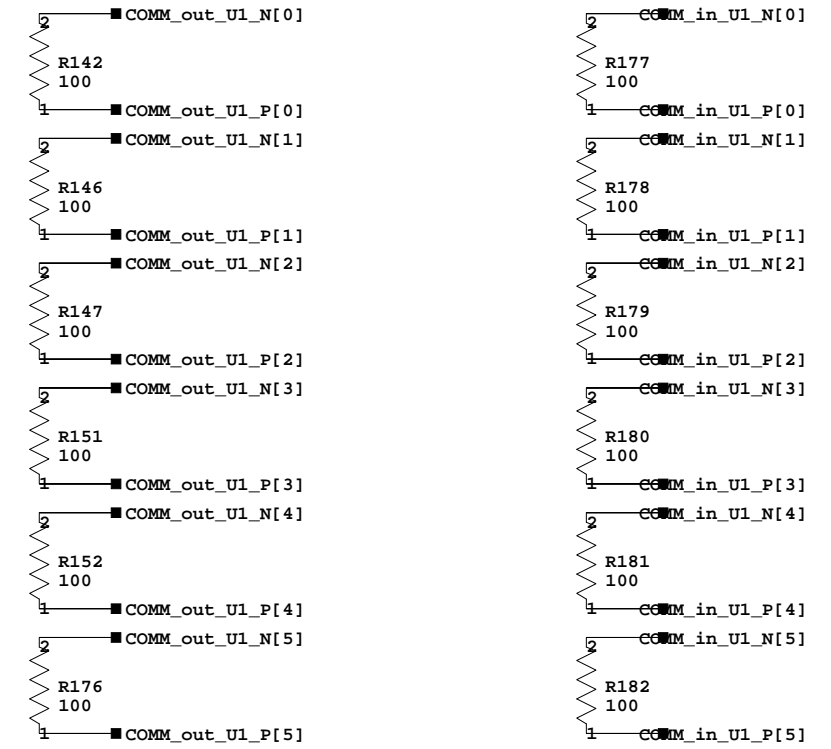
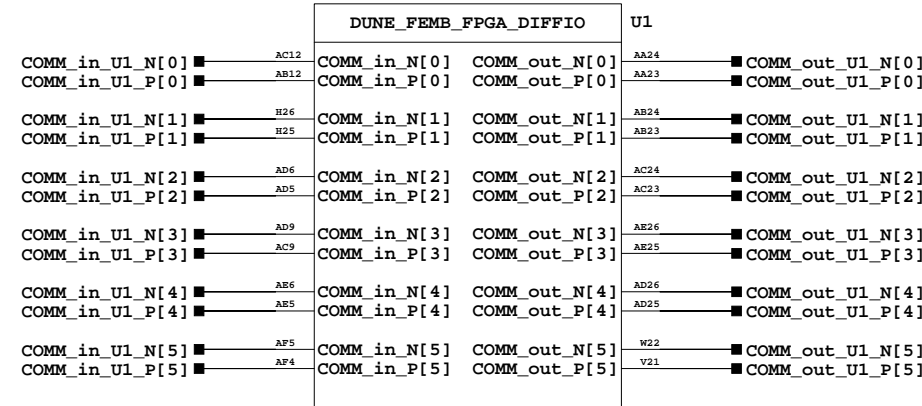
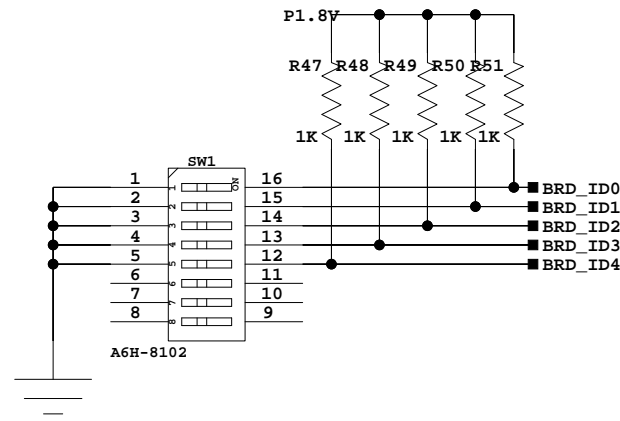




UNDER FPGA



LVDS TERMINATION LVDS TERMINATION
PLACE UNDER FPGA U1 PLACE UNDER FPGA U2

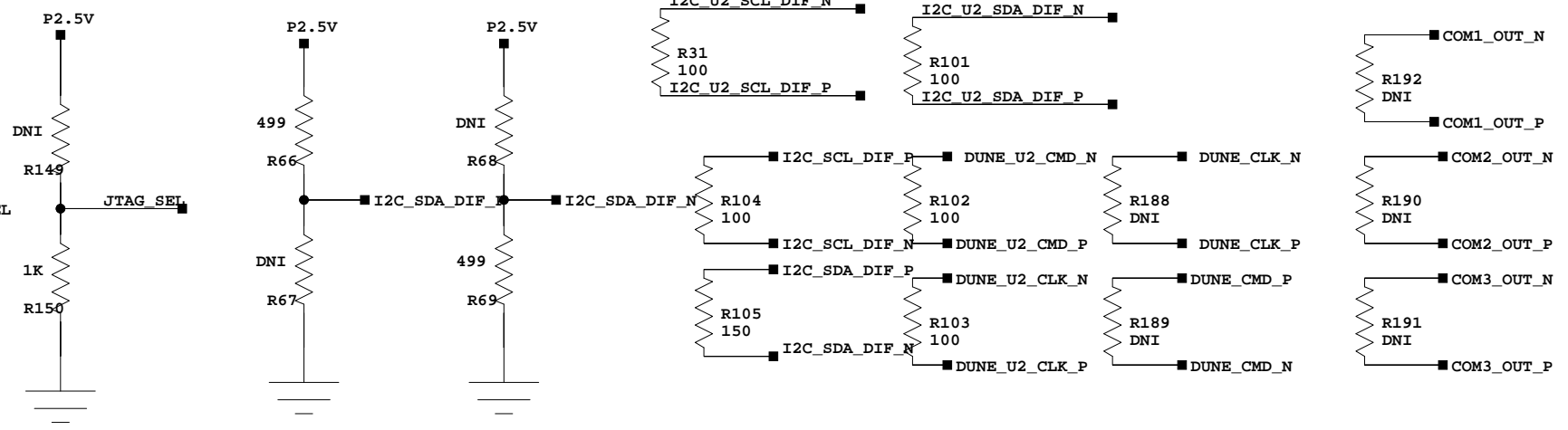
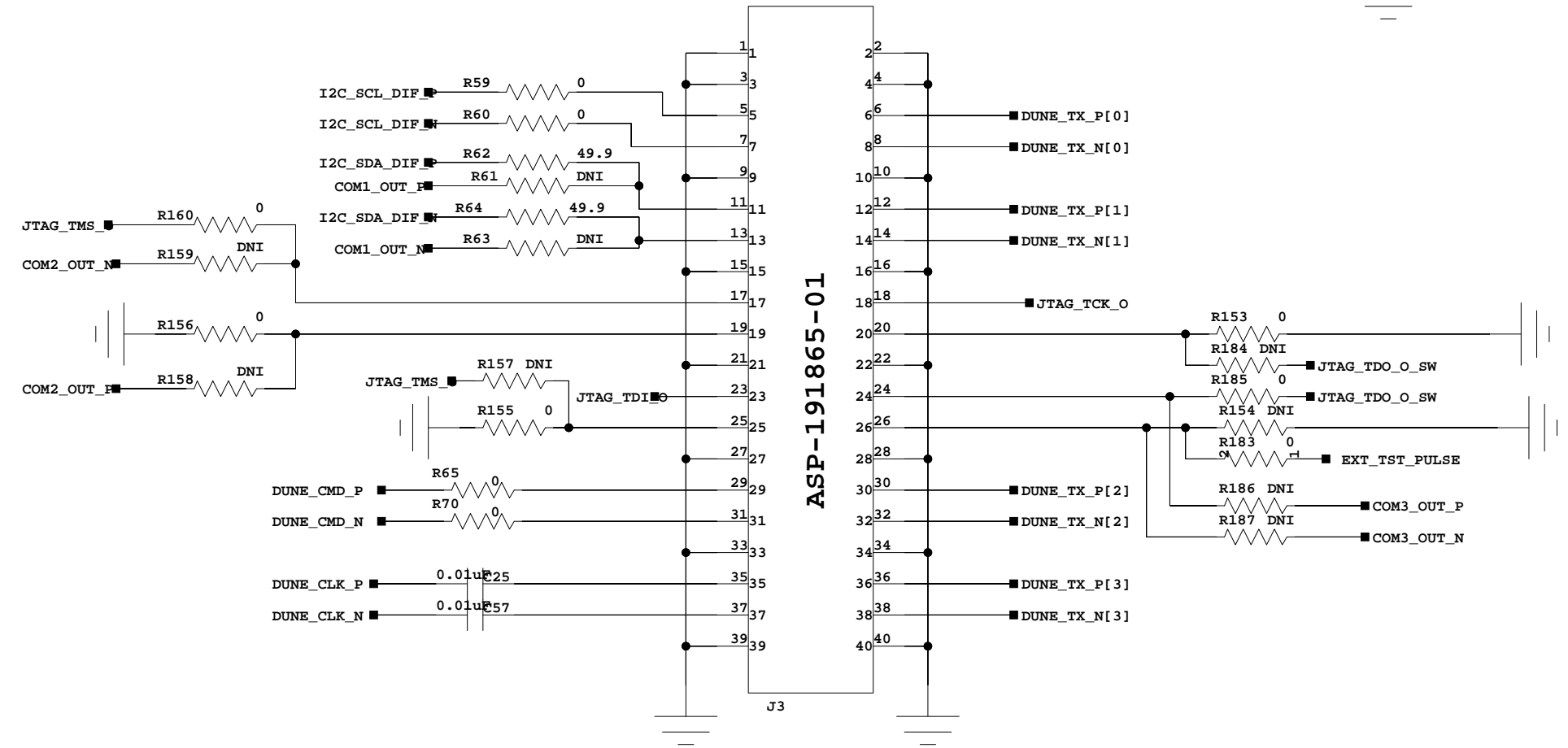
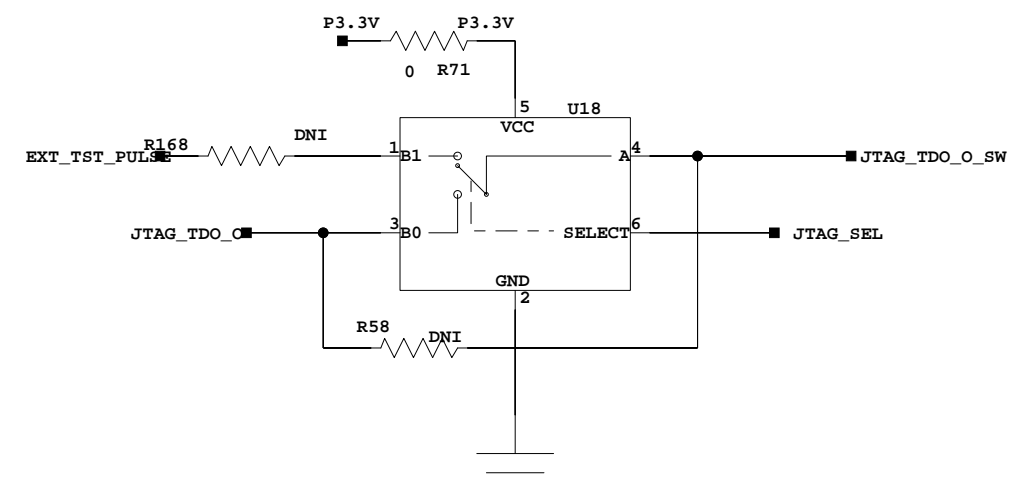
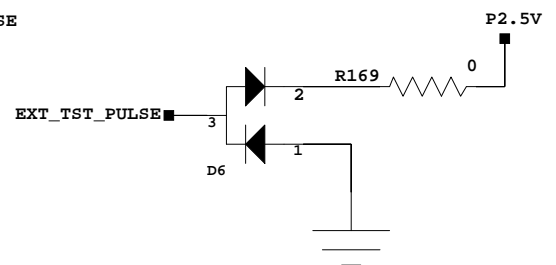
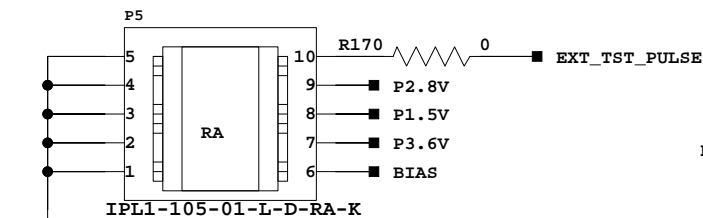
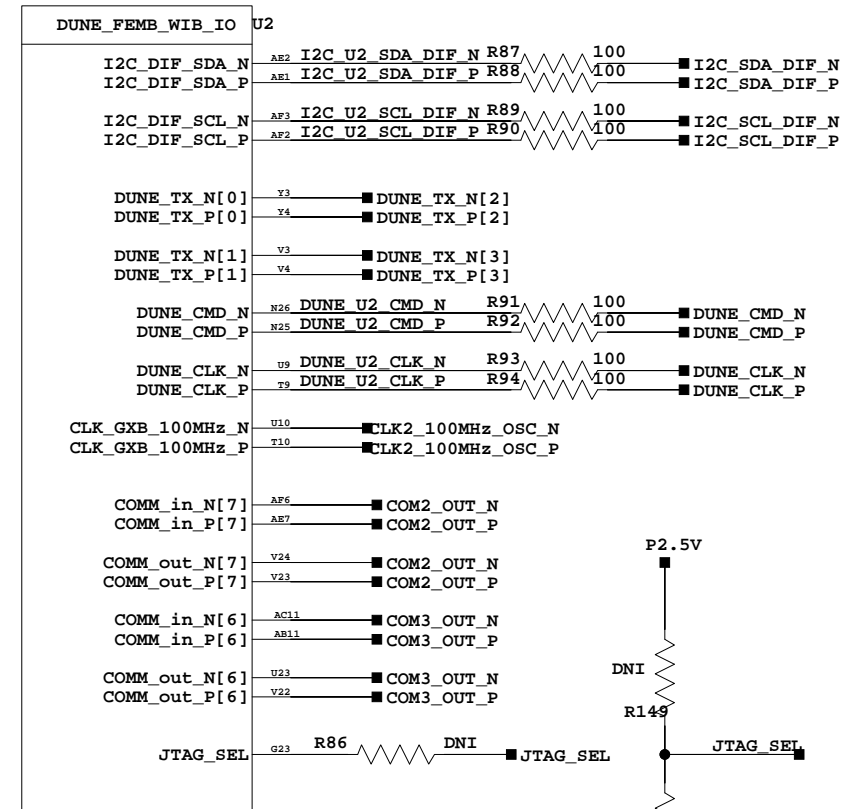
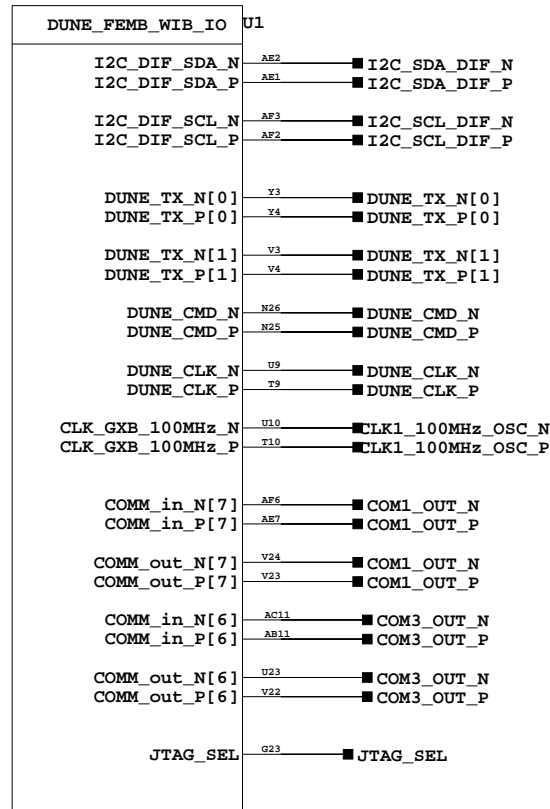


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DUNE_MISC_IO

Date: 10/12/2019:09:27

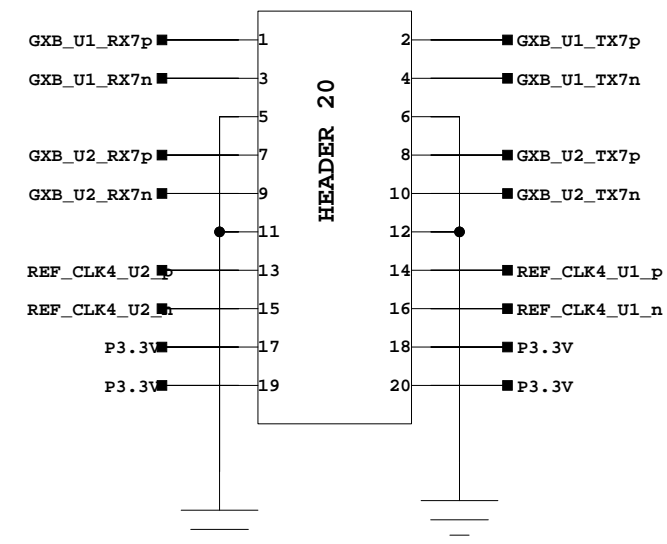
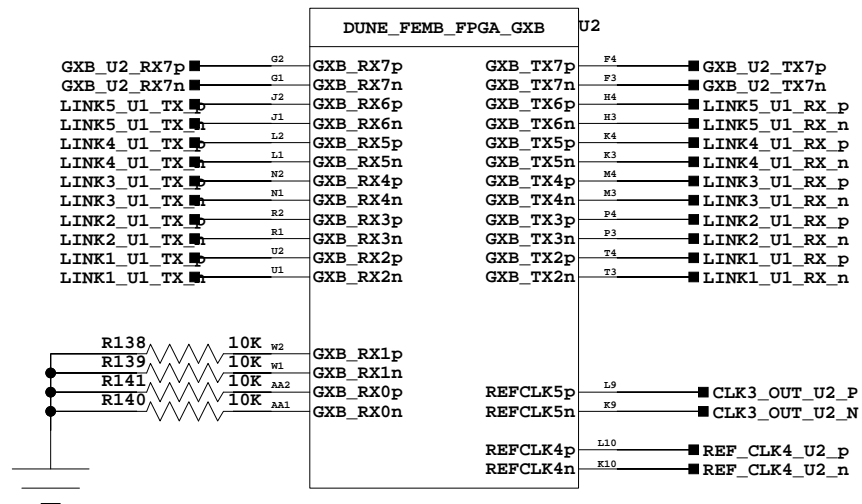
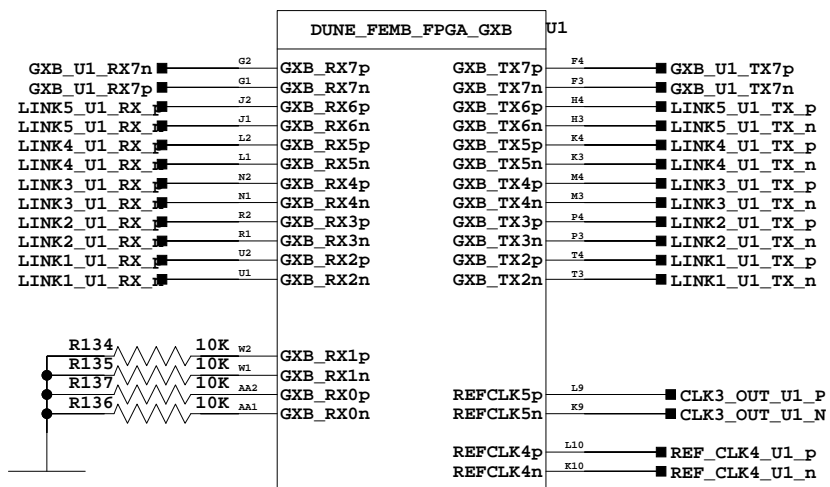
DRAWN BY: Jack Fried



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DUNE_FPGA_IO

Date: 10/12/2019:09:27 DRAWN BY: Jack Fried

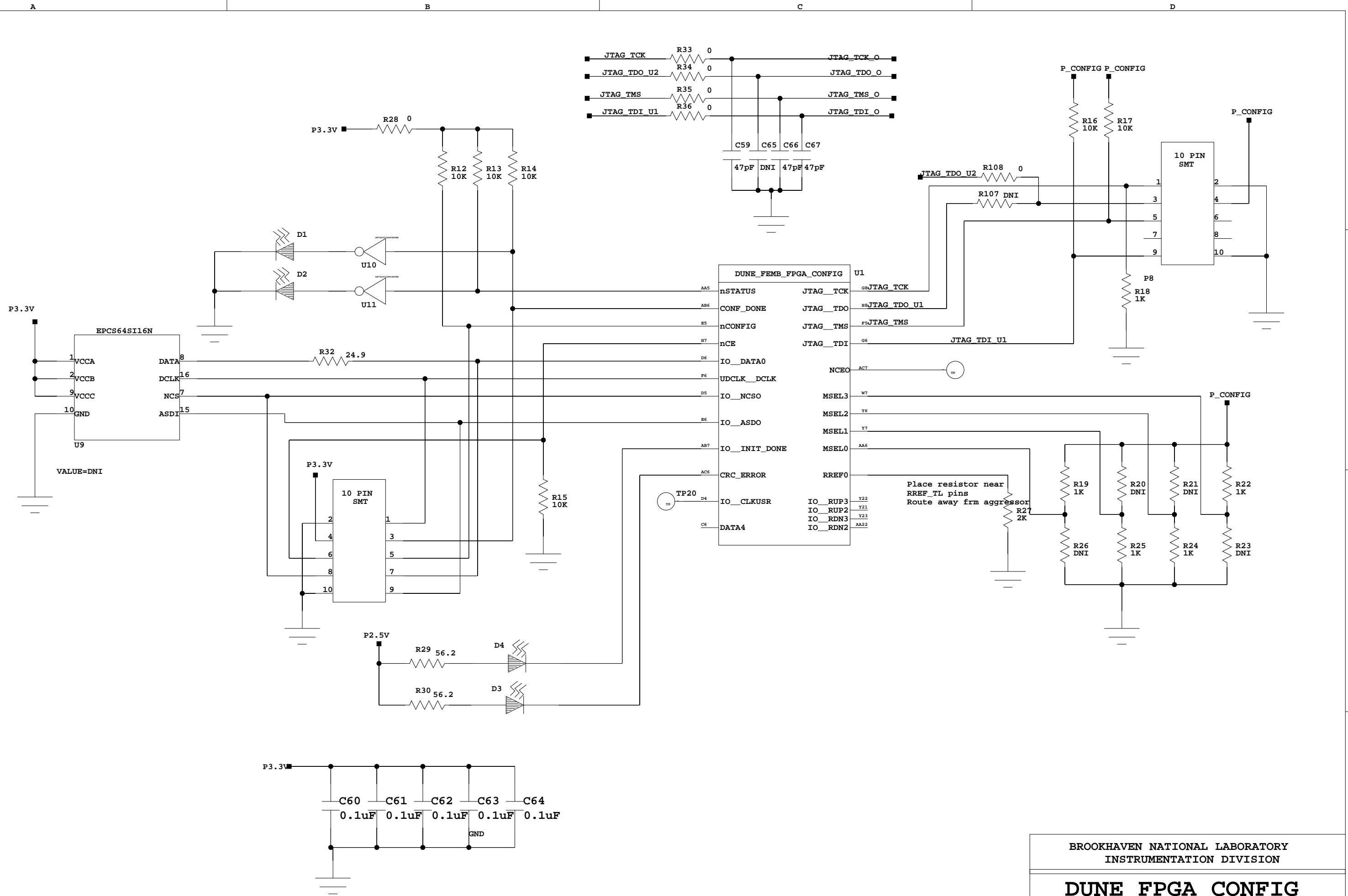


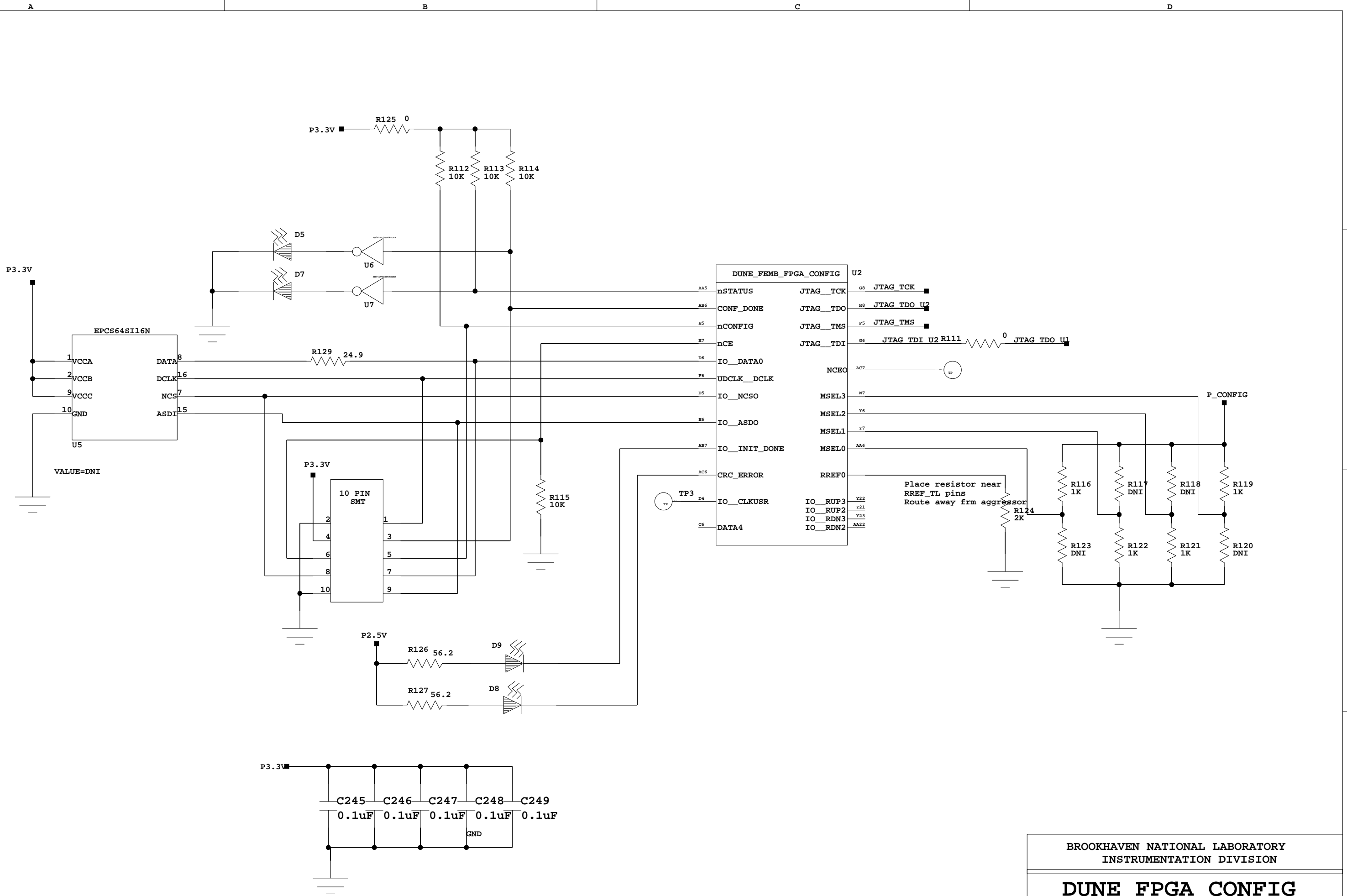
BROOKHAVEN NATIONAL LABORATORY
INSTRUMENTATION DIVISION

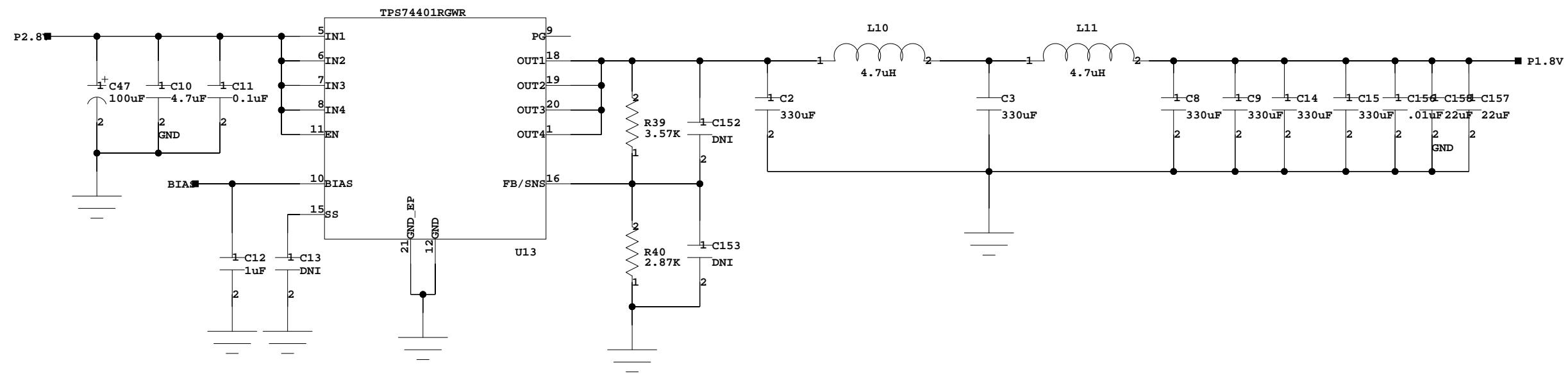
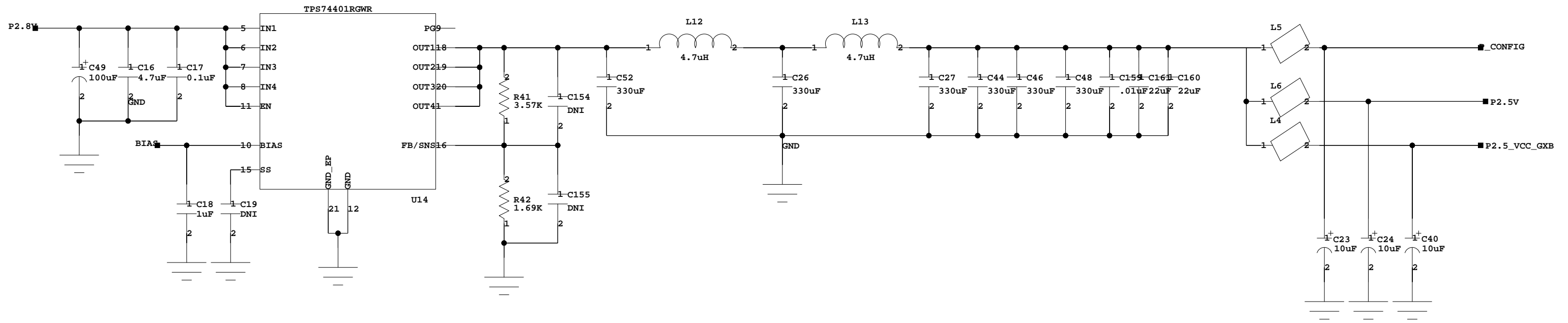
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Date: 10/12/2019:09:27

DRAWN BY: Jack Fried





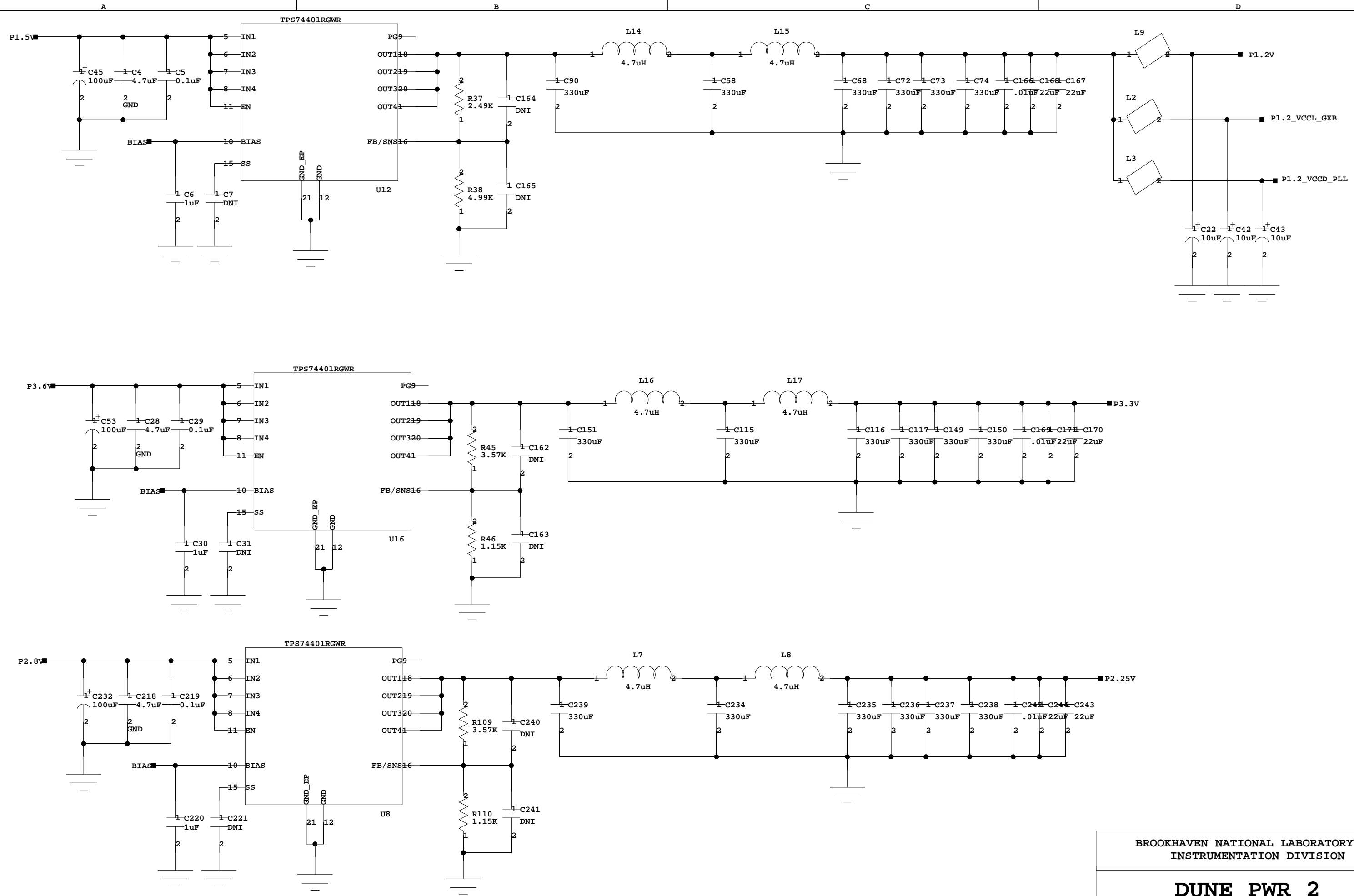


BROOKHAVEN NATIONAL LABORATORY
INSTRUMENTATION DIVISION

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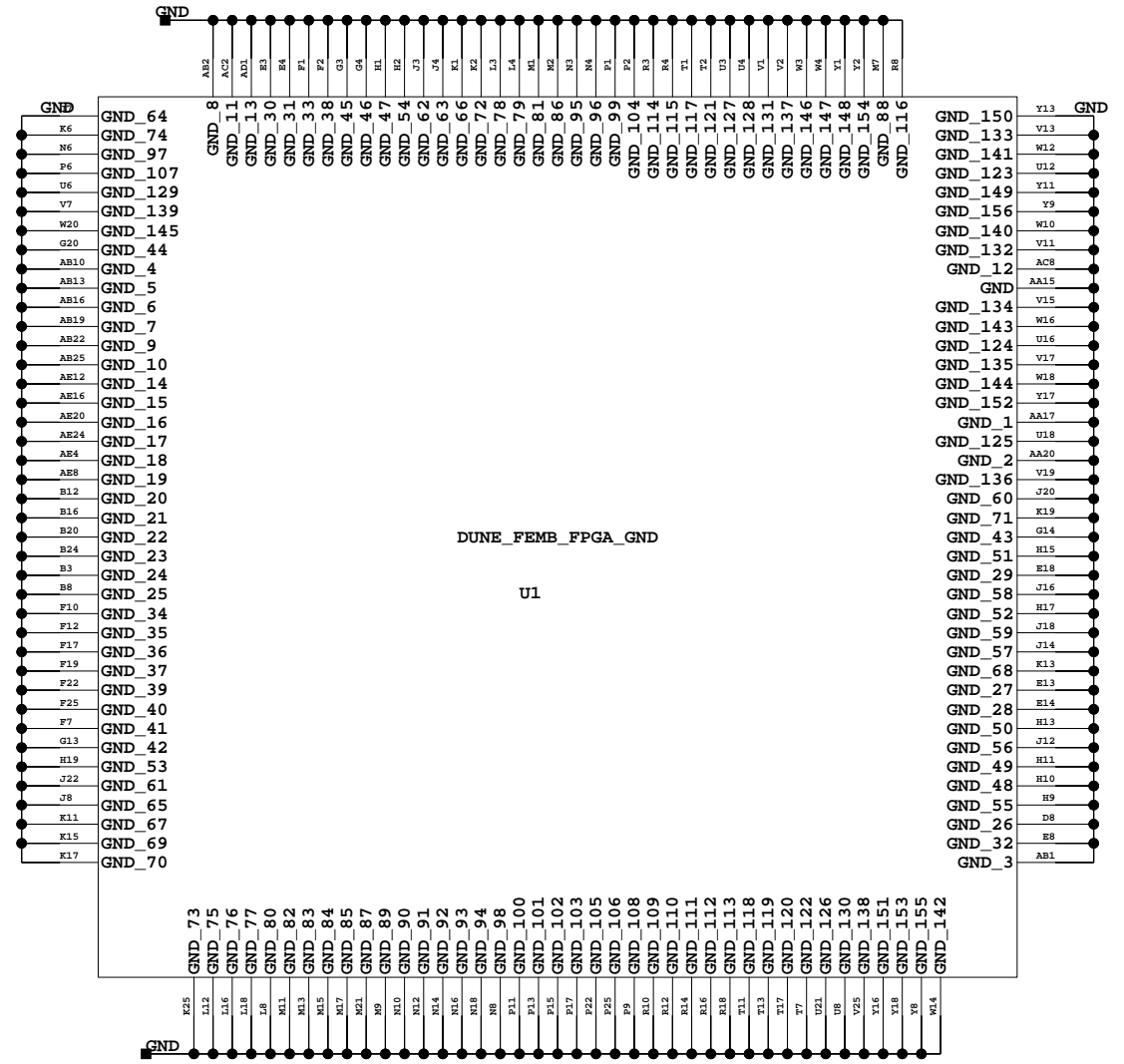
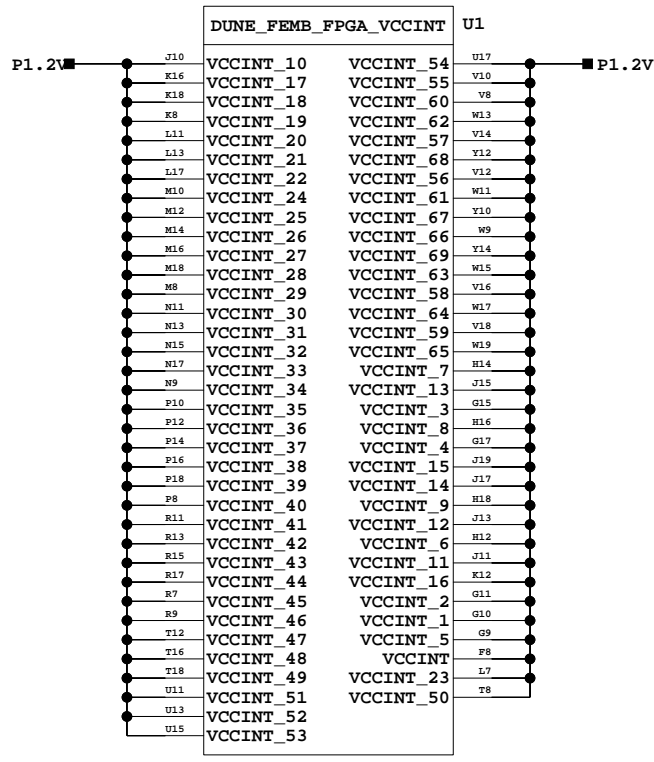
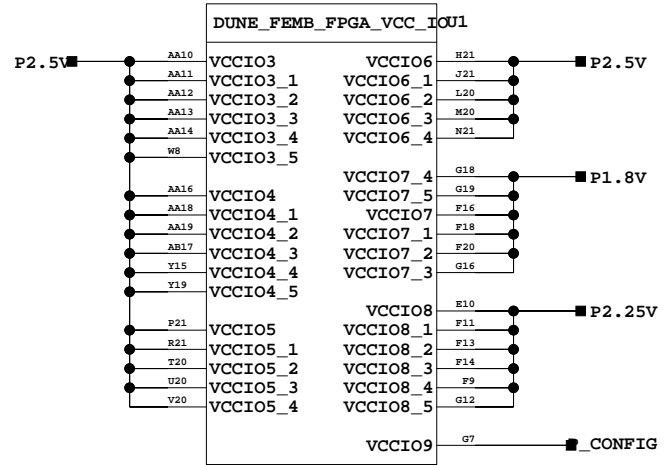
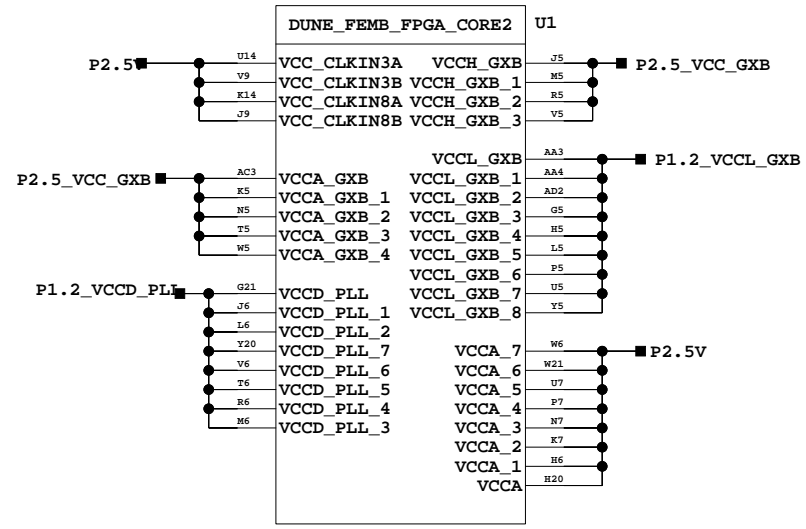
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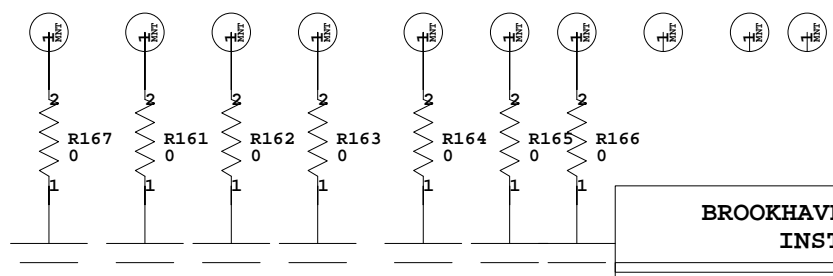
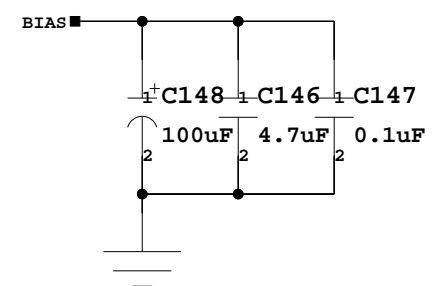
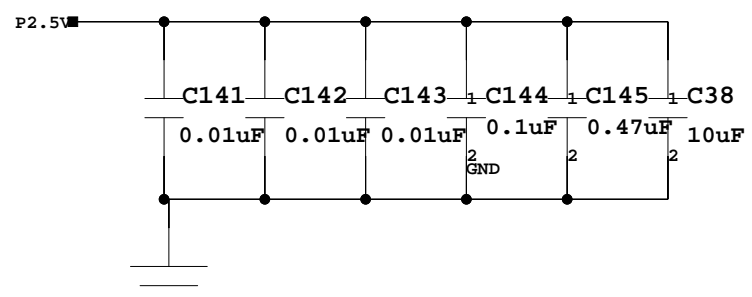
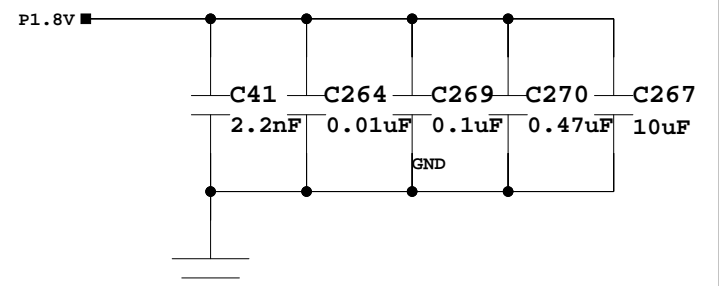
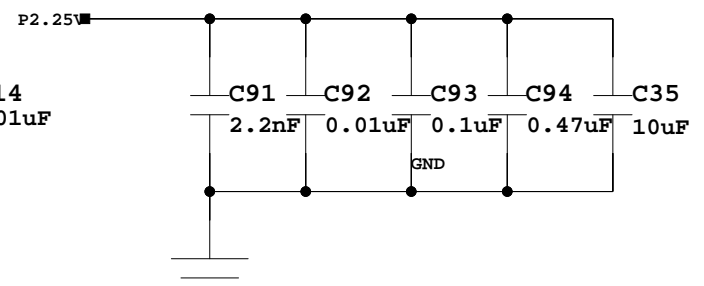
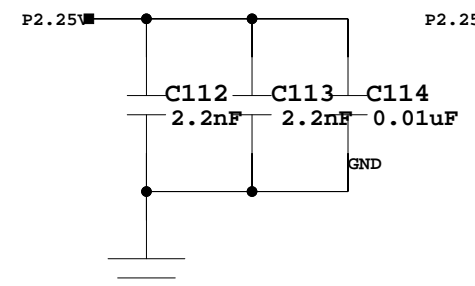
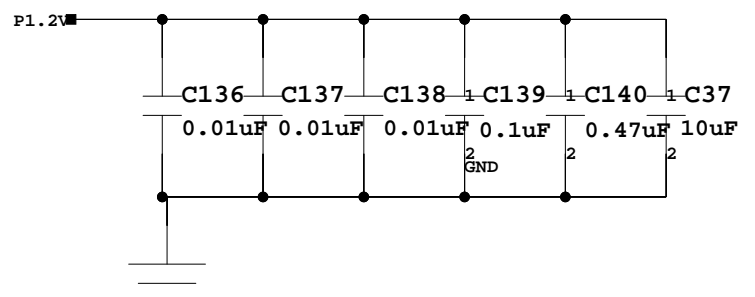
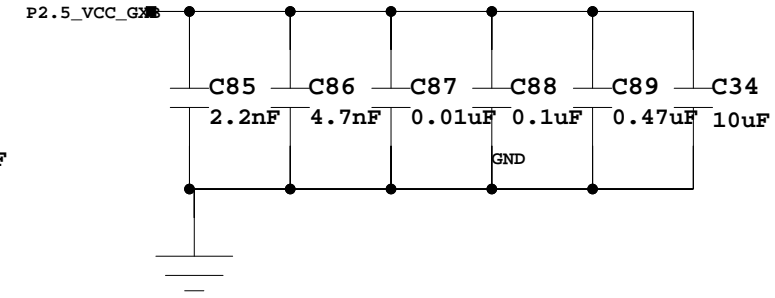
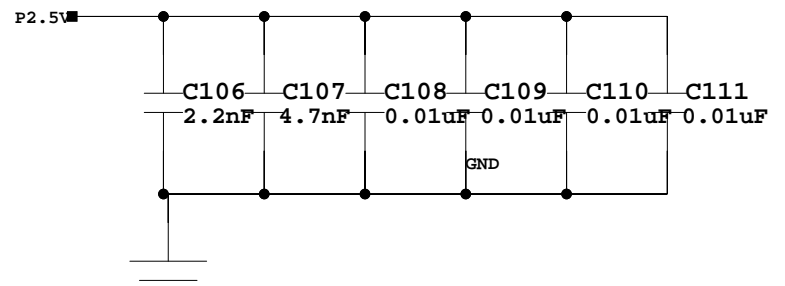
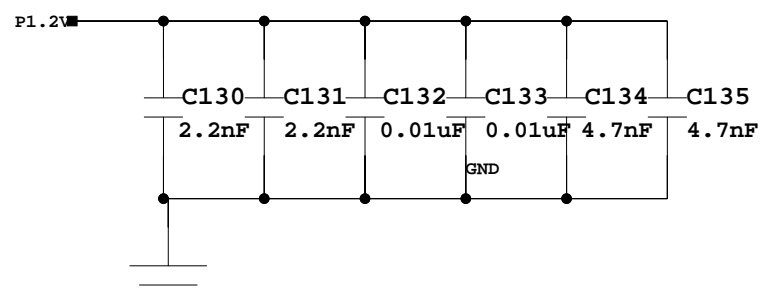
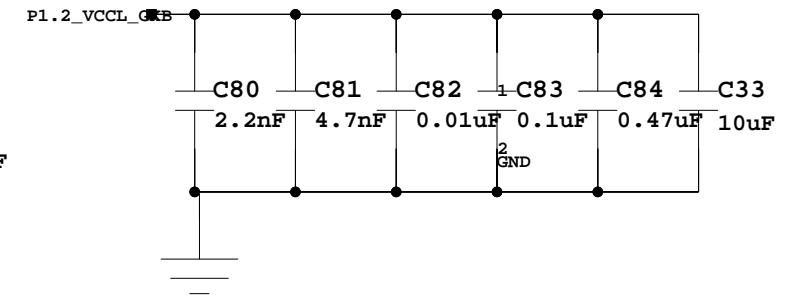
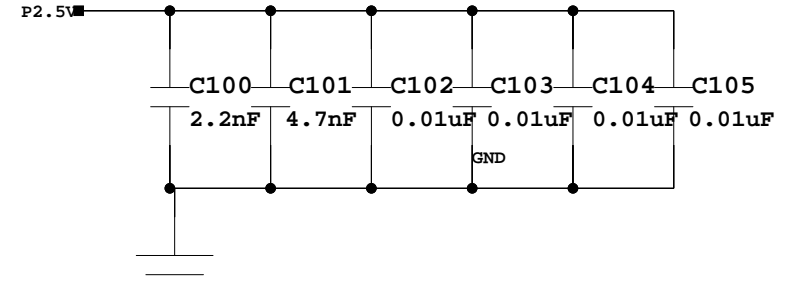
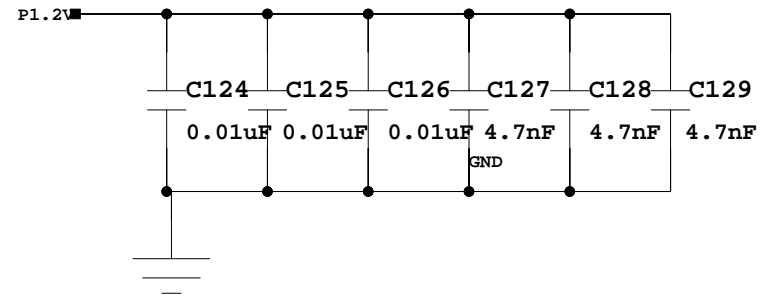
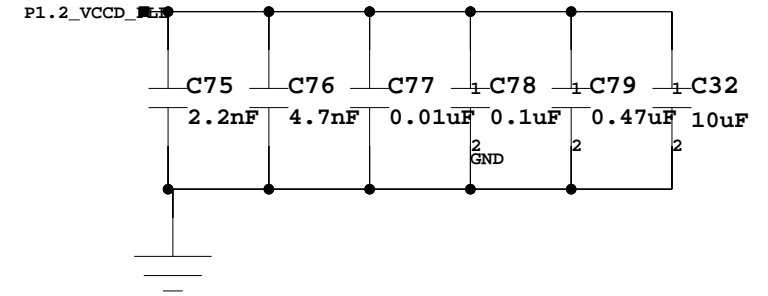
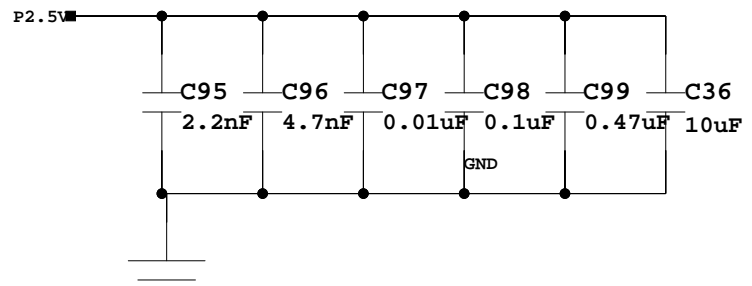
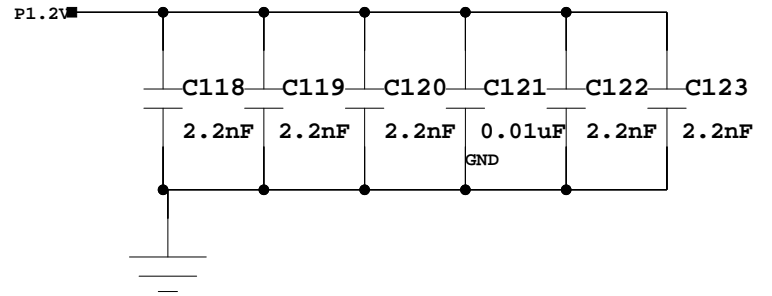


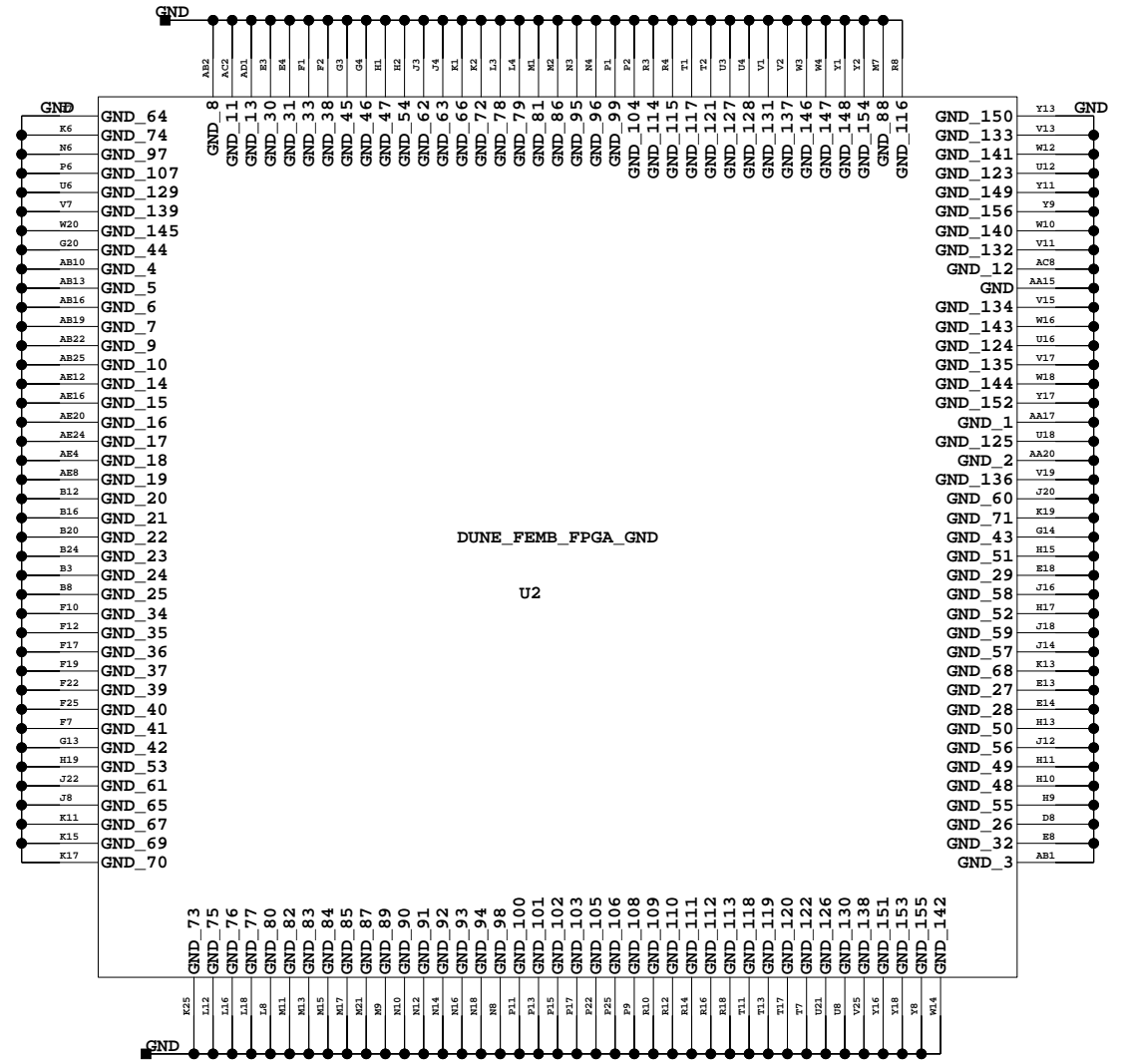
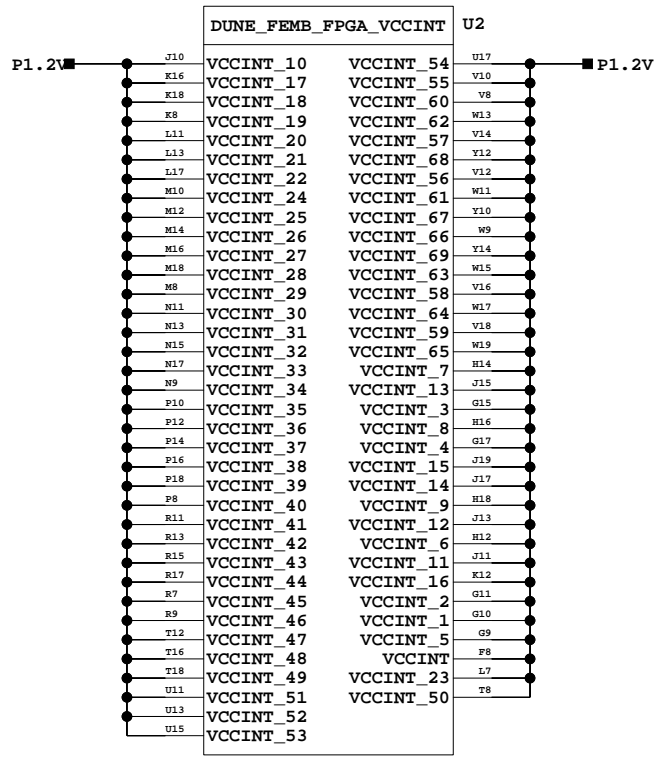
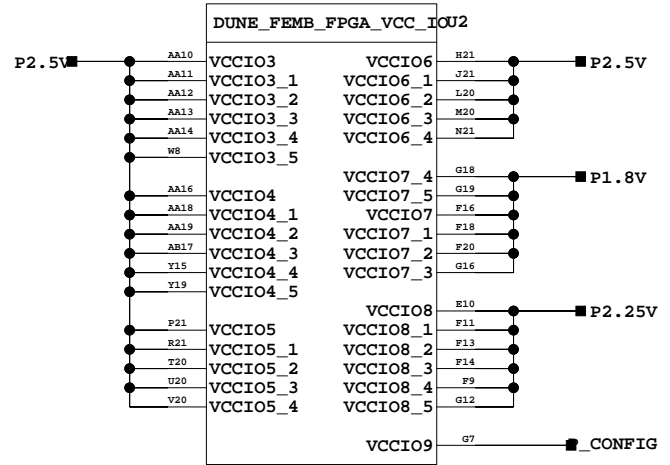
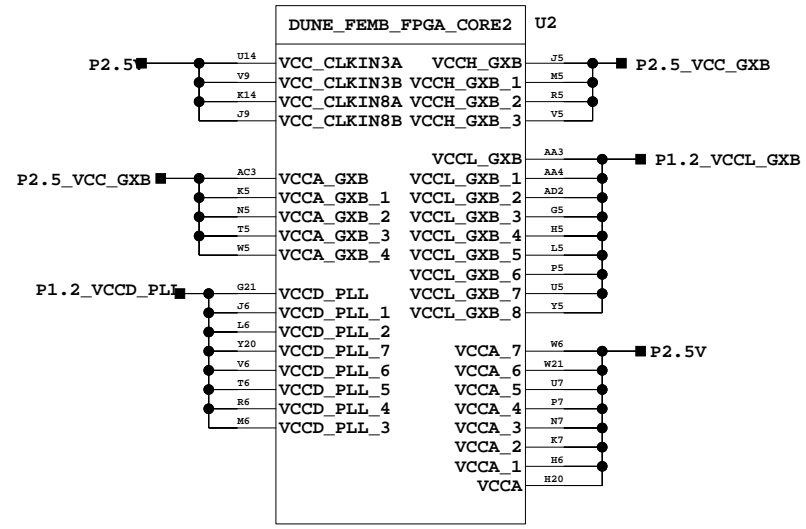
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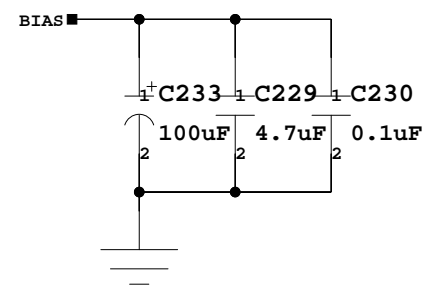
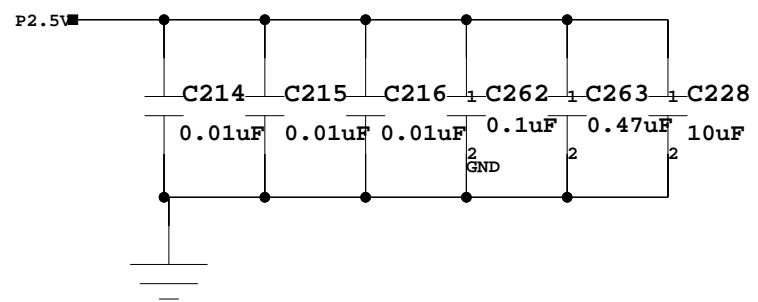
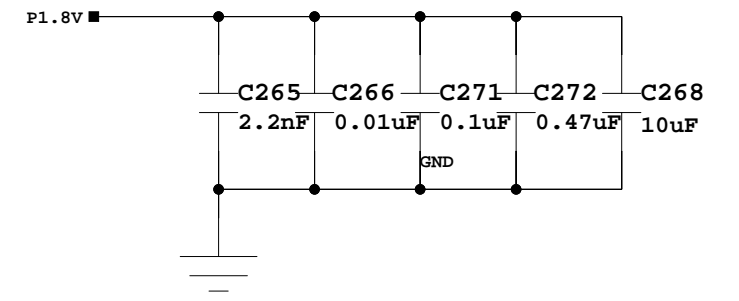
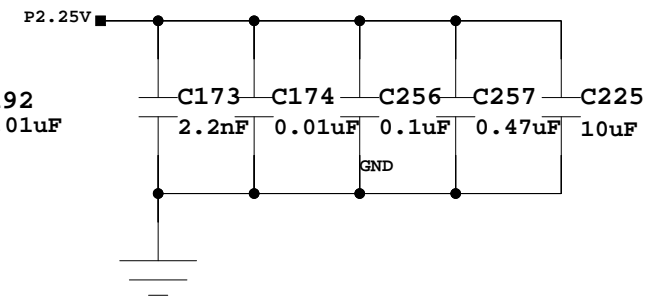
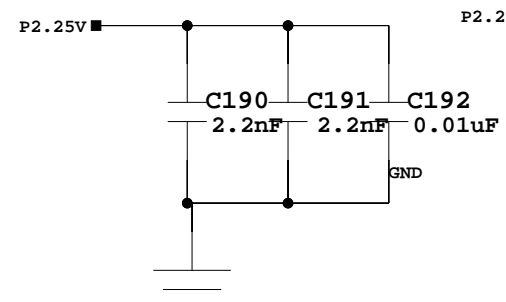
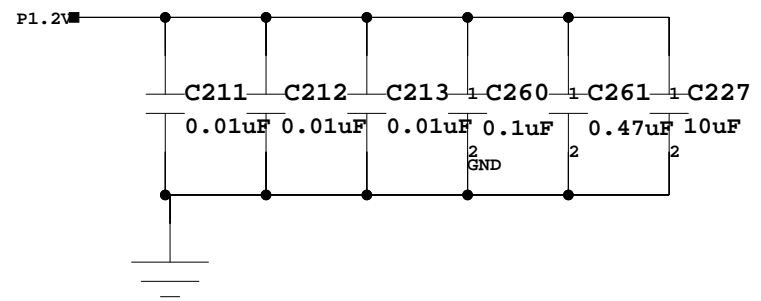
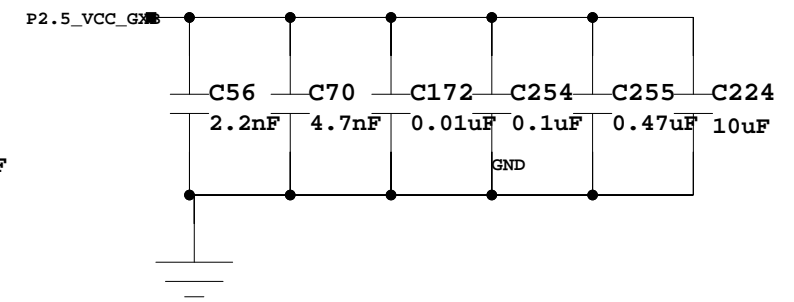
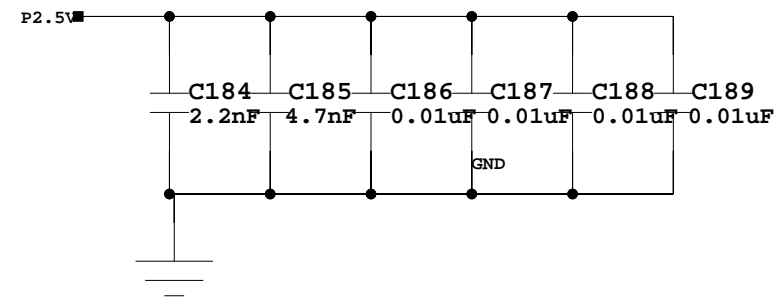
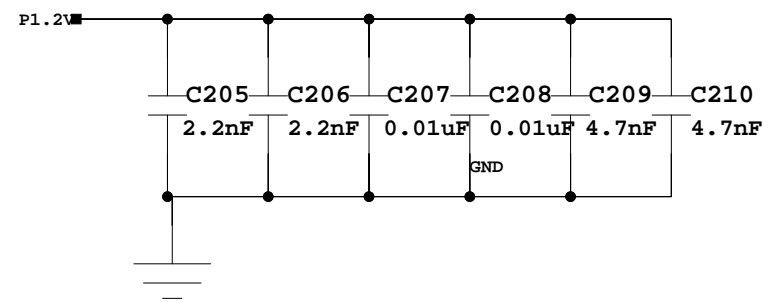
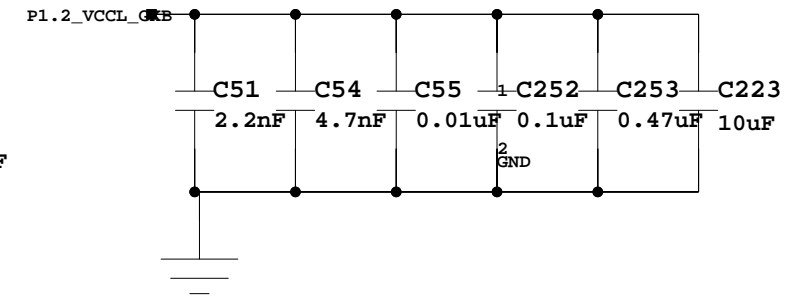
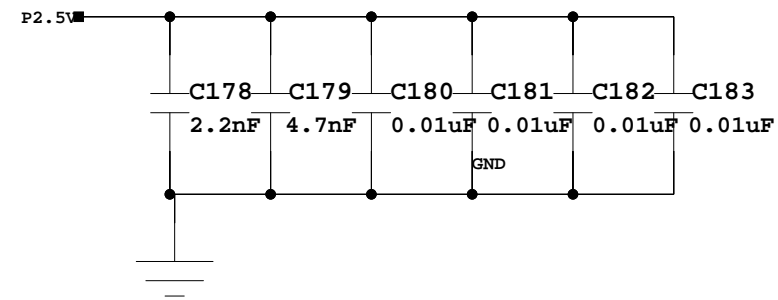
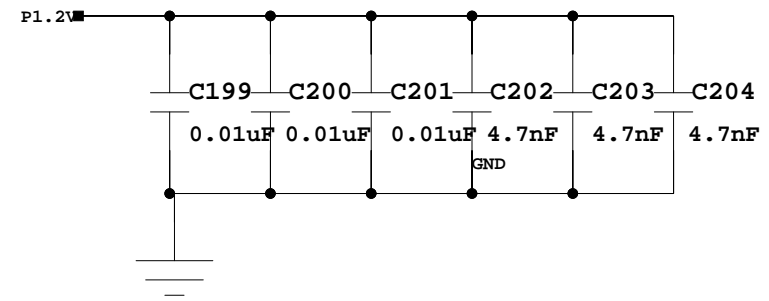
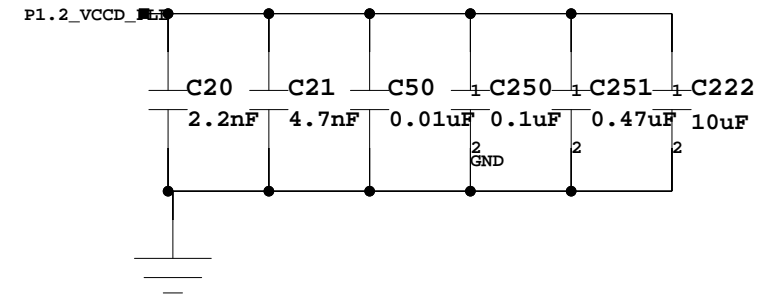
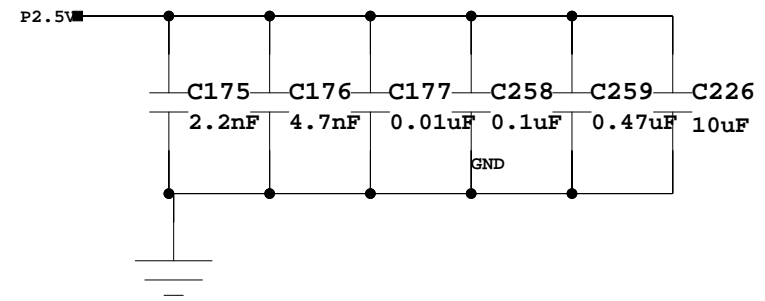
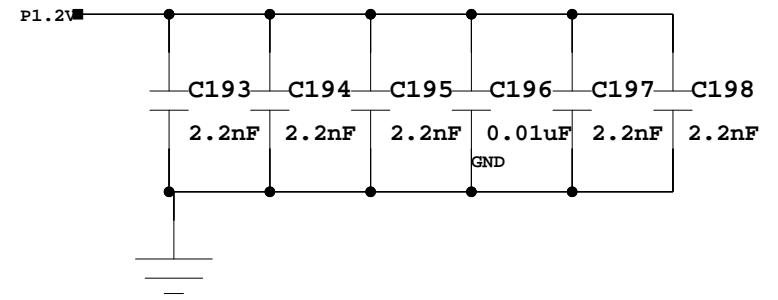




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